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FINAL ENGINEERING REPORT
FOR

ADAPTIVE BEAMFORMING (ABF) SYSTEMS DESIGNER'S HANDBOOK STUDY

This report covers the period
12 June 1972 to 12 May 1973

TEXAS INSTRUMENTS INCORPORATED
Advanced Systems Department
Equipment Group
P.O. Box 6015
N. Central Expressway
Dallas, Texas 75222

DEPARTMENT OF THE NAVY
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Code 90114

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ABSTRACT

This report summarizes the results of a study conducted for the Navy to develop an Adaptive Beamforming (ABF) Systems Designer's Handbook to aid sonar system planners and designers in conducting tradeoff analyses of such variables as size, weight, power and complexity versus system capability. Tasks involved in this study, which are summarized in this report, include algorithm definition, system design, semiconductor tradeoff analyses, system implementation, and handbook and module specification generation. Summary charts and equations relating design parameters to system size, weight, power, and complexity are conveniently tabulated in appendix form for ease of use by the sonar system designer.

ADAPTIVE BEAMFORMING (ABF) SYSTEM DESIGNER'S HANDBOOK STUDY

PART I

1.0 PURPOSE

Adaptive Beamforming (ABF) has been shown to provide significant improvement in sonar system performance over conventional beamforming techniques for a wide range of applications. Subsequently, advanced planning in many systems includes consideration of ABF for backfit into existing sonar systems and for inclusion in new systems. Many of these systems are intended for mobile platform applications where size and weight are critical factors. System planners must consider these and a number of other factors when performing tradeoffs involving system design.

The purpose of this study was to develop for the Navy an *Adaptive Beamforming (ABF) Systems Designer's Handbook* which is designed to aid Navy sonar system planners and designers in conducting tradeoff analyses of variables such as system size, weight, power and complexity versus system capability. System capability is defined in terms of implementation variables such as the number of input channels, the number of output beams, data bandwidth, algorithm, data and computation precision, and filter length. Inherent in accomplishing the purpose of this study has been the definition of common building block modules for ABF systems, specifications for which have been included in the appendix of this report.

2.0 RESULTS

2.1 Technical Approach

The approach taken to generate the *ABF Systems Designer's Handbook* was to develop a system architecture that was partitionable into common building block modules, the number of which could be expanded or contracted to accommodate a realistic range of system implementation variables. Inherent in this approach was the goal of minimizing the number of modules and the number of module types required; usually, these two goals cannot be met simultaneously. Arriving at the best choice of system partitioning involves such considerations as circuit technology, packaging technology, and the total number of systems to be built which impact recurring and nonrecurring costs per module. Because of the large number of possible combinations of values of implementation variables considered, a great deal of engineering experience and judgment was used in the final selection of the best method of system partitioning in the modules.

Development of the *ABF System Designer's Handbook* was accomplished in five distinct tasks. These were:

Algorithm Definition

System Design

Semiconductor Tradeoffs

System Implementation

Handbook Generation and Module Specification.

Efforts under these tasks are summarized in the following paragraphs, which deal with technical activity.

A number of technology and design tradeoffs were addressed in performing these various tasks. The key issues addressed as part of system design were the flexibility required of the system and the type of memory elements to be employed. Under semiconductor tradeoffs, basic component technologies were examined as well as the complexity of devices, (that is, small-, medium-, and large-scale integration). Packaging tradeoffs to include the type of printed circuit board used and the type of semiconductor component packaging (for example, DIPs, flat packs, and beam leads) were studied relative to their impact on system size, weight, power and complexity. Once the system design and the various technologies were identified, specifications for common building block modules were generated. Based on this information, charts and equations, showing various design parameters were assembled for ease of use by the sonar system designer. Both of these items are summarized in appendix form for ease of reference.

2.2 Technical Activity

2.2.1 Introduction

Technical activity under the ABF Systems Designer's Handbook Study was divided into five separate task areas which were: algorithm definition, system design, semiconductor tradeoff, system implementation, and handbook generation and module specification. The following paragraphs of this section discuss the technical activity under each of these tasks and present the results of each.

2.2.2 Algorithm Definition

2.2.2.1 General

There are two basic types of ABF algorithms, deterministic (matrix inversion) and gradient search (stochastic approximation). These are illustrated in Figure 1. Both may be implemented in either the time or frequency domain. Most off-line data analysis work is accomplished using the deterministic technique because it is well-understood theoretically and is cost-effective to perform on general-purpose computers. However, gradient search schemes have proved more desirable for real-time systems implementation for a number of reasons, the most important of which is reduced system complexity. For this reason, the study program has concentrated on the time domain gradient search algorithm.

2.2.2.2 Algorithm Specification

Within the scope of time-domain stochastic approximation algorithms to be considered, two basic classes of algorithms were defined for implementation studies. These were:

Class I: Constrained Approach

Class II: Unconstrained Approach.

As used in this report, the terms "constrained" and "unconstrained" refer to constraints placed on the algorithm to preserve signal. In the constrained case, the algorithm is "constrained" to preserve signal from the desired look direction, and unconstrained implies that no constraint on signal preservation is specified in the algorithm.

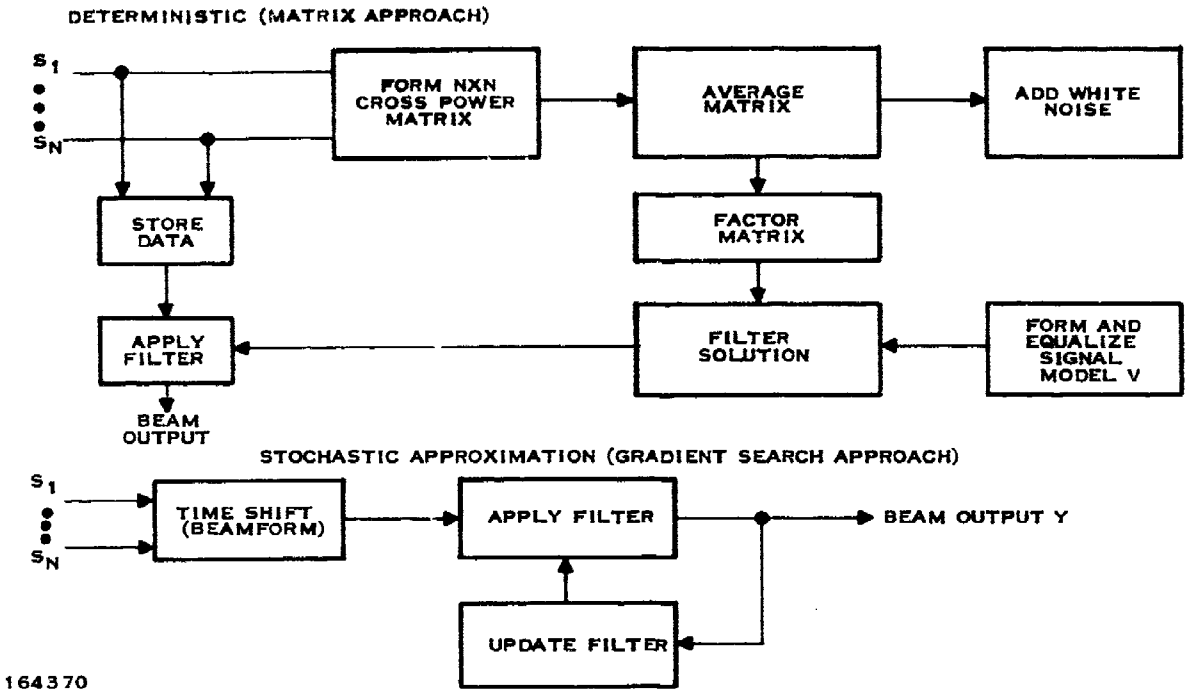

Figure 1 – ABF Algorithms.

The exact implementation of the algorithm was specified by the technical monitor at Naval Underwater Systems Center, New London. It was agreed that a single generalized algorithm which covered both constrained and unconstrained cases would be used. The agreed upon algorithm is Equation (64) of reference 2, which is:

$$W(n+1) = \left(I - \frac{1}{K} DD^T\right) [W(n) - 2\mu X_A(n)Y(n)] \qquad (1)$$

where

$W(n)$ = adaptive filter weights

I = an identity matrix of dimension $L \times L$, where L = filter length or number of adaptive weights

K = number of sensors

D = matrix to produce signal content in the data from a single channel signal

μ = convergence rate parameter

$X_A(n)$ = array data to be used in forming the adaptive beam

$Y(n) = Y_M(n) - Y_A(n)$, the ABF beam output

$Y_M(n)$ = the main array beam steered output for the n*th* data point

Y_A 1/A(n) = the auxiliary array output for the n*th* data point.

Class I and Class II algorithms were then defined as being, respectively, the constrained and unconstrained versions of Equation (1); that is, with the term $1/K\ DD^T$ nonzero or zero.

2.2.2.3 Implementation Variables

Two algorithms were included in the handbook and a number of variables were considered for the handbook to be of general use to the system designer. These variables were:

- Number input channels
- Number output channels
- Length of filter
- Bandwidth of data (i.e., sample rate)
- Frequency of filter update
- Precision.

There are seven different variables that must be considered if the type of algorithm is included in the list. Each of these parameters represents a tradeoff area that must be considered when designing the ABF system. The handbook includes tradeoff data for each of these parameters.

The range of variables that should be considered was defined in conversations between Texas Instruments and NUSC/NL personnel. These are summarized below.

- The number of input channels, N_i, was defined as the number of adaptive channels. Values of N_i for the two classes of the algorithm are:

  Class I: 8, 16, 32, 64, 128

  Class II: 1, 2, 4, 8

- Number of output beams, N_o

  Class I and II: 1, 2, 4, 8, 16, 32, 64, 128

- Length of filter, L:

  Class I and Class II: 2, 16, 32, 64, 128

- Sampling rate, F_s, for Class I and Class II: 0.5, 2.5, 5, 10 and 25 kHz
- Frequency of update, U:

  Class I and Class II: 1, 1/2, 1/4, 1/16, 1/64, 1/128

- Precision in bits, P, for Class I and Class II:

  Data precision, P_x = 4, 8, 12

  Filter precision, P_f = 4, 8, 12, 16

  Filter update precision, P_u = 8, 12, 16.

All multiply operations will be $P_x \times P_x$. The study was confined to the filter design and application subsystem of the general ABF system: that is, the inputs will be bulk-delayed hydrophone outputs or the beamformed outputs, and no bulk time data delaying is considered.

Out of the total possible number of cases, the following cases of special interest were defined to be given particular attention during the study.

Class I

Case 1: $N_i = 16$; $N_o = 32$; $F_s = 5$ kHz; $L = 128$
$P_x = 12$ bits; $P_f = 16$ bits; $P_u = 16$ bits; $U = 1, 1/2$

Case 2: Same as Case 1, except $N_i = 32$

Case 3: Same as Case 1, except $N_i = 64$

Class II

Case 1: $N_i = 1$; $N_o = 64$; $L = 128$; $F_s = 25$ kHz
$P_x = 8$ bits; $P_f = 12$ bits; $P_u = 12$ bits; $U = 1/64$

Case 2: Same as Case 1, except $N_i = 2$

Case 3: Same as Case 1, except $N_i = 4$.

2.2.3 System Design

2.2.3.1 Algorithm

The first step taken toward defining a system architecture was to rearrange the generalized algorithm in a sequence optimized in the sense of minimizing the number of required stored-data memory cycles. For this purpose, adaptive filter weights and array data are considered to be stored data. This results in the following sequence of equations, which will be implemented by the selected architecture.

For the constrained case, the first part of the sequence is to compute the beam outputs and to apply the constrained condition to the filter weights. This gives the equations

$$Y_o^t = YM_o^t + \sum_k \sum_l [X_{klo}^t \ (W_{klo}^t - A_{lo}^t)] \tag{2}$$

$$W_{klo}^t = W_{klo}^t - A_{lo}^t \tag{3}$$

The second part of the sequence is used to compute beam outputs after the constrained conditions have beem satisfied. This gives

$$Y_o^t = YM_o^t + \sum_k \sum_l [X_{klo}^t \ (W_{klo}^t)] \tag{4}$$

Finally, the filter update part is given by

$$W_{klo}^{t+1} = [W_{klo}^t + (2\mu Y_o^t) \ X_{klo}^t] \tag{5}$$

$$A_{lo}^{t+1} = \sum_k \frac{1}{k} W_{klo}^{t+1} \tag{6}$$

where

Y = the ABF beam output

YM = the main array beam-steered output

X = array data to be used in forming the adaptive beam

W = unconstrained adaptive filter weights

A = average unconstrained filter weights

W = constrained adaptive filter weights

μ = convergence rate parameter

k = input channel number

l = filter point

o = output beam number.

2.2.3.2 Processing Requirements

The processing throughput rate required for the various cases of special interest was defined to establish a system architecture approach that would be compatible with the problem and to determine the feasibility of implementing the ABF system within the NAFI SHP constraints. The total number of operations per second is related to the implementation variables by the following equation where a single operation is typically a combined subtract, multiply, and accumulate process.

$$OPS/SEC = N_i\, N_o \times F_s \times L \times (1 + \mu) \qquad (7)$$

The processing throughput requirements for the various cases of special interest are tabulated in Table 1. The requirement of up to some 2.5 billion operations per second is formidable and suggests an architecture of parallel processing elements (PE) with dedicated hardware for this class of problems.

TABLE 1 – PROCESSING THROUGHPUT REQUIREMENT.

	Operations Per Second $\times 10^6$	N_i	N_o	F_s (kHz)	L	U
Class I						
Case 1	655	16	32	5	128	1
Case 1A	492	16	32	5	128	1/2
Case 2	1,311	32	32	5	128	1
Case 2A	983	32	32	5	128	1/2
Case 3	2,621	64	32	5	128	1
Case 3A	1,966	64	32	5	128	1/2
Class II						
Case 1	208	1	64	25	128	1/64
Case 2	416	2	64	25	128	1/64
Case 3	832	4	64	25	128	1/64

2.2.3.3 System Configuration

The system approach considered consists of a hardwired architecture using special-purpose hardware tailored to the given algorithm. This approach defines a minimum

hardware baseline system which is analyzed to determine the technical feasibility of implementation within the constraints of NAFI SHIP. With this configuration, only incidental modifications to the algorithm are programmable.

The system configuration for the Class I, Case 1 example of interest is given in Figure 2. This configuration represents a processor with a single instruction stream issued by the PE Ensemble Controller (EC) and a multiple data processing capability within the array of PEs. The multiple data processing approach to the ABF problem demands some partitioning of the problem between the various PEs in the array. Possible dimensions for the partitioning considered include the output beams, the input channels, and the filter points. Each PE may be assigned some part of the total ABF problem which would involve the processing required for some combination of output beams, input channels and filter points. The implications of the three dimensions of partitioning are discussed in the following paragraphs.

Output beams provide the cleanest break for partitioning from the standpoint of data flow and maintainability, since data parameters are not fed from one output to another. Therefore, partitioning of each PE to operate on only one output beam becomes the first cut at partitioning.

The next cut at partitioning was by the input channel allocation to each PE. In this case, it was determined that it is desirable to process all input channels within each PE without partitioning because any partitioning by input channels would necessitate the summing of partial results of the average of unconstrained filter weights at each point of the filter length for each input sample. This would require additional special hardware in each PE.

The next cut at partitioning was by filter length. In this case, each PE is assigned only a section of the filter for processing, with a sufficient number of PEs configured to cover the complete length. A final summation of partial beam outputs formed by the various PEs is required to complete the process. However, this summation is a relatively simple process which can be accomplished with little overhead cost.

The processing throuhput capability of the system configuration is now considered. For this, the PE circuit speed is assumed to be sufficient to permit four million arithmetic operations per second where each operation is a combined substract, multiply, add and accumulate process. This rate is judged to be obtainable within the SHP constraints by using PE implementation with TTL circuit technology and a pipeline structure. The pipeline structures increases total throughput rate for vector operations by inserting holding registers between the logic stages of the PE. Using the partitioning described for the Class I, Case 1 problem of special interest and the PE throughput rate of four million operations per second, the total processing time required for the beam output and the filter update is 193 microseconds. The time allocation for these computations is tabulated in Table 2 and is seen to be within the sample time interval of 200 μs for the 5-kHz sample rate. The time allocation for instruction propagation is made to allow the control signals associated with each new instruction of the sequence to propagate to all the PEs before the next clock pulse is received. This time allocation is necessary for control purposes because of the central controller feeding a large number of PEs packaged within several racks of equipment. At this point, the question of each PE operation requiring additional time for propagation must be considered. The answer is that most instructions are executed many times without any control signal change and that the data flow paths within a PE or between two PEs will be well-controlled as to propagation delays. Thus, this system approach provides optimum clock speeds for the various processing conditions.

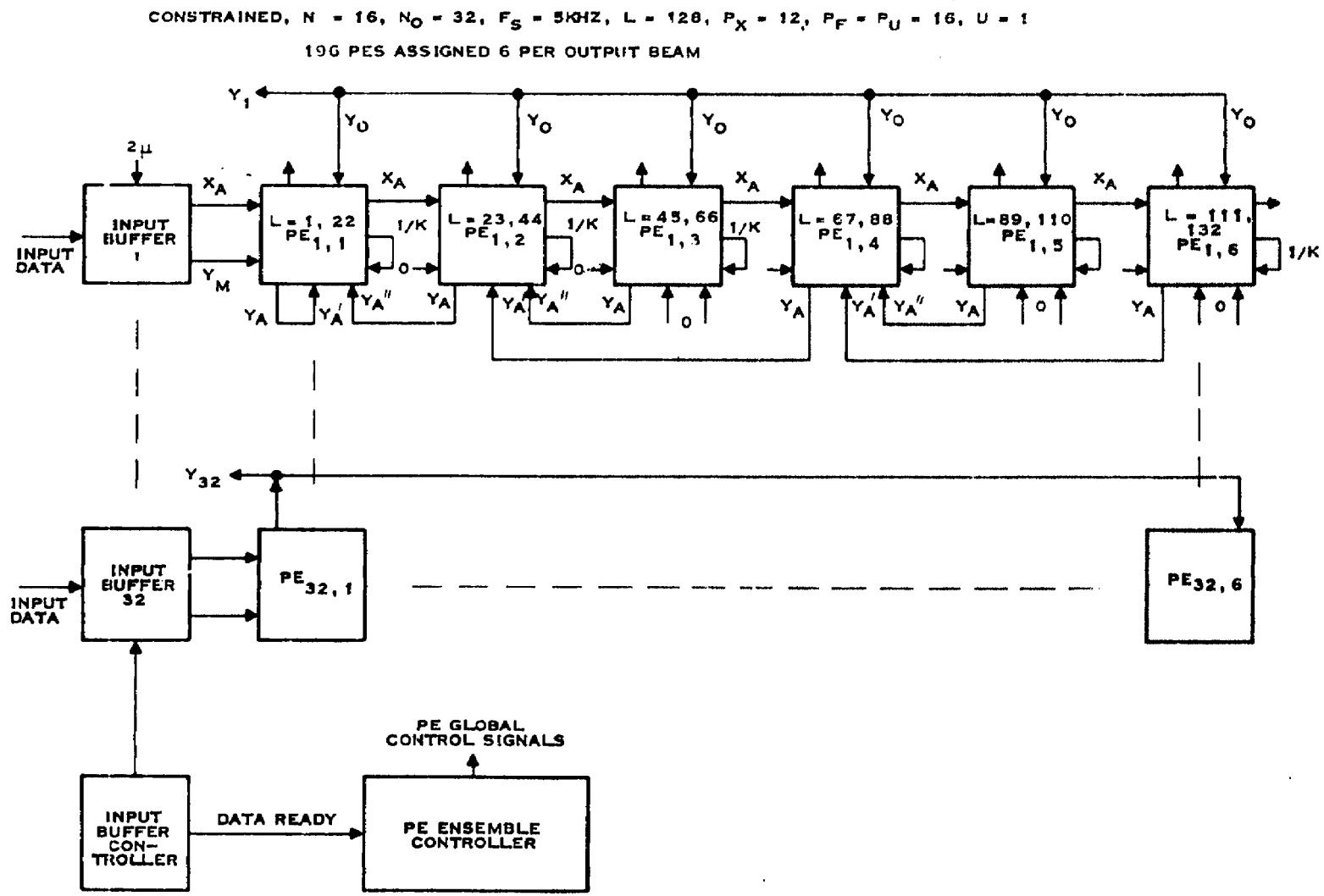

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Figure 2 – ABF System Configuration for Class I, Case 1, System of Interest.

TABLE 2 - PROCESSING TIME ALLOCATION FOR CLASS I, CASE 1 PROBLEM.

Function	Operations	Time (μs)
Output Beam Form		
Load pipeline	5	1.25
Accumulate partial beams	352	88
Sum partial beams	4	1
Instruction propagation	25	6.25
Filter Update		
Compute $2\mu Y_o$	4	1
Load pipeline	5	1.25
Accumulate average weights	352	88
Instruction propagation	25	6.25
Total	772	193

TABLE 3 – SYSTEM CONFIGURATIONS FOR SPECIAL CASES.

	PE Array	PE Partitioning			
	Row x Column	L	N_i	N_o	Total PEs
Class I					
Case 1	32 x 6	22	16	1	192
Case 1A	32 x 4	32	16	1	128
Case 2	32 x 12	11	32	1	384
Case 2A	32 x 8	16	32	1	256
Case 3	32 x 22	6	64	1	704
Case 3A	32 x 16	8	64	1	512
Class II					
Case 1	64 x 1	128	1	1	64
Case 2	64 x 2	64	2	1	128
Case 3	64 x 4	32	4	1	256

Using the technique of partitioning and time allocation described for the first problem of special interest, suitable system configurations were established for each of the defined cases of special interest. The results are tabulated in Table 3, which shows the number of PEs required for implementing each of the cases of special interest. In the configuration, only one PE controller is required for any one of the cases. However, two controliers could be used if it is desirable to split the ABF problem into two PE arrays. This would have only minor impact on hardware complexity.

2.2.3.4 Processing Element

The design of the PE was considered in detail because these units represent the vast majority of hardware in the ABF system. From the system configuration study of special cases, up to 704 PEs and one controller are required in a single ABF system. Therefore, the PE design is readily seen to be the most critical for a practical system.

Figure 3 is the block diagram of a PE designed for use in the Class I, Case 1 problem. This PE design with some change to the length of the shift regsiter memories, is applicable to all the cases of special interestst. However, the complexity of the PE can be reduced for implementing the Class II problem by removing the indicated blocks used only for the constrained case. The following considerations were made to minimize the complexity of the PE.

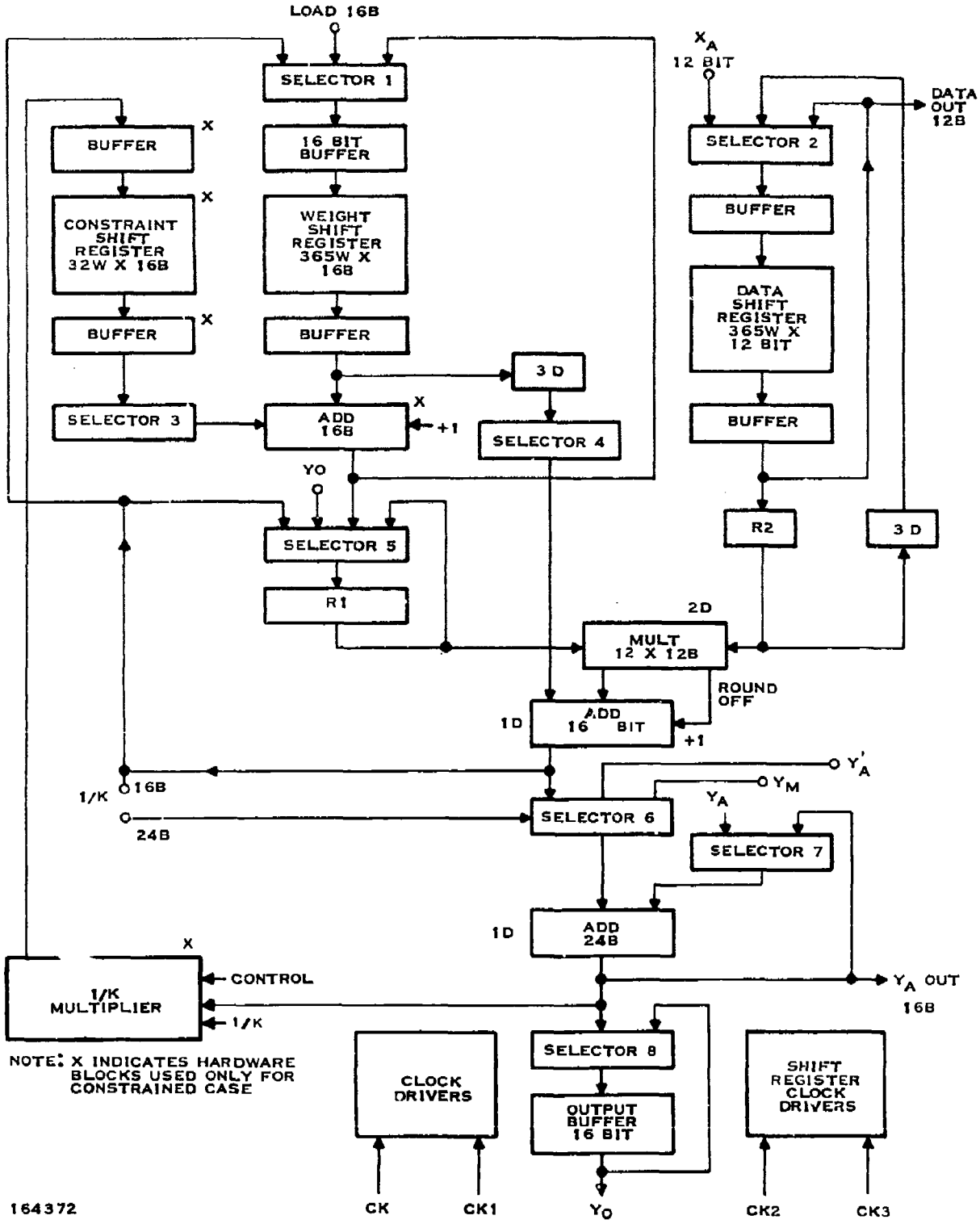


Figure 3 – Processing Element.

The PE structure is based on a pipeline architecture which allows a clock rate or 4 MHz for processing. For the initial design, TTL circuit technology was assumed and a worst case logic delay of 150 nanoseconds was allowed between registers. This delay includes register setup and delay time so that at least 100-ns wiring progapation time is allowed for signal transfer. The arithmetic structure of the PE is noted to be a wired subtract, multiply, add and accumulate operation with selectable gating for problem steering. The main memories are shift registers, with one for data and one for filter weights. Provisions are included to pass on part of the data memory contents to the next PE in the filter length chain. This is required because of the partitioning by filter points. Provisions are also included for the complete sum of the partial beam outputs through the inputs Y_A^I and Y_A^{II}.

2.2.3.5 Processing Element Ensemble Controller

The primary function of the PE Ensemble Controller is to provide the source of instruction sequence for solving the ABF problem. The controller is shown in block diagram form in Figure 4.

The controller is similar to most computer controllers in the sense that it contains a program memory and program counter. The program memory will be implemented with PROMs since program modifications will not be required for any particular system configuration. In fact, with suitable modifications to the contents within the program memory, this PE Ensemble Controller is applicable to all system configurations for the ABF problem.

The controller departs from normal computer controllers in that no operand addresses are required. This is because the data (operands) within the PEs are stored in shift registers with no provisions for addressing. However, the special feature of two hardware loops are implied with each instruction. There are an instruction repeat counter that allows any instruction to be repeated by the designated number of times, and a loop repeat counter that allows a group of instructions to be repeated as a do loop by the designated number of times. The capabilities are implemented in the instruction format so that no execution overhead time is required to set up and control either loop. The operation of these loops and the permissible branches may be better understood by studying the instruction format shown in Figure 5.

The idle/run state controller is used to synchronize the ABF system to the sampling rate of input data. The control states are shown in Figure 6. Processing is initiated from the idle state whenever the data ready signal is received. Then, processing is terminated by executing the instruction containing a run tag set to "one." Provisions are included for receiving two data ready signals before the next run tag. This may occur during the filter update process for update frequencies less than one.

The typical program sequence for the ABF problem is shown in Figure 7. This is seen to be a very short program of only 14 instructions; however, it is adequate with the built-in loop provisions previously described. The arrows in the figure indicate loop paths to be executed.

2.2.4 Semiconductor Tradeoffs and System Implementation

System implementation depends on the semiconductor technology selected since for a given packaging technique such as SHP, the board packaging limitations of the number of pins, number of ICs, and power dissipation change the IC count per board, depending upon device

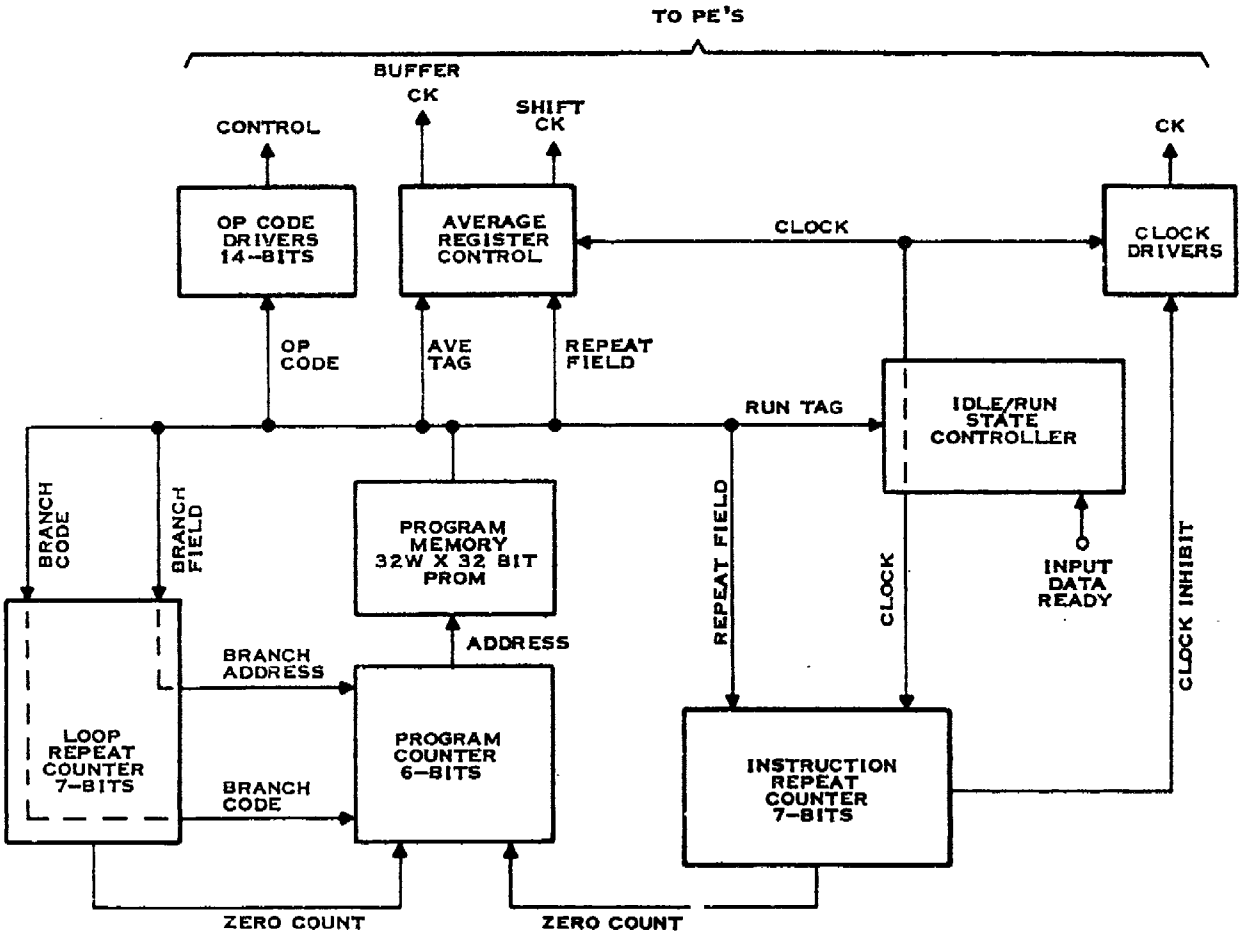


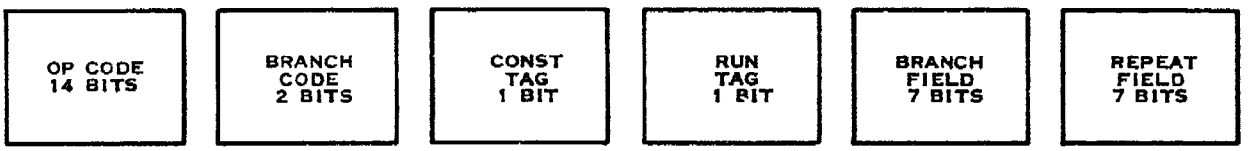
Figure 4 – Processing Element Ensemble Controller.

complexity and power dissipation per gate. For this reason, the semiconductor technology selection must be considered in concert with system partitioning.

The packaging technology studies, board partitioning, component technology implementations and final semiconductor selection are discussed in the following paragraphs.

2.2.4.1 Packaging Technique

The general guidelines adopted for the study were to use the standard hardware program (SHP) packaging if at all possible. Initially, it was believed that SHP might provide some limitations because of the potentially large size of the ABF system for certain high computational problems. A brief analysis of SHP versus large multilayer boards (MLB) was conducted.



NOTES:

BRANCH CODE

00	NO BRANCH. EXTEND REPEAT FIELD TO INCLUDE BRANCH FIELD.
01	SET LOOP COUNTER TO VALUE IN BRANCH FIELD
10	BRANCH TO LOCATION DESIGNATED BY BRANCH FIELD AND DECREMENT LOOP COUNTER IF CONTENTS OF LOOP COUNTER IS NOT ZERO
11	UNCONDITIONAL BRANCH TO LOCATION DESIGNATED BY BRANCH FIELD

CONSTRAINT TAG

0	REPEAT INSTRUCTION THE NUMBER OF TIMES DESIGNATED BY REPEAT FIELD.
1	CLOCK BOTH CONSTRAINT REGISTER BUFFERS, THEN ADVANCE SHIFT REGISTER BY DESIGNATED NUMBER WITHIN THE REPEAT FIELD. EXECUTION OF OTHER INSTRUCTIONS PROCEEDS AFTER BUFFER TRANSFER; THEREFORE, PROGRAM FAULT RESULTS IF NEW EXECUTION OF THIS INSTRUCTION IS REGISTERED BEFORE PREVIOUS EXECUTION IS COMPLETED

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Figure 5 – Instruction Format.

The MLB used in the Texas Instruments Advanced Scientific Computer (ASC) was selected as the sample board on which the analysis was to be performed. Table 4 is a summary of the results of this comparison. The integrated circuit packaging density (ICs per cubic foot) was used as the criterion for tradeoff analysis. Two types of components packages were studied: dual-in-line packages (DIPs) and flat packs. Maximum and typical densities were investigated as part of the study. Maximum density refers to the maximum number of components that could be mounted on a

TABLE 4 – COMPARISON OF BOARD-LEVEL PACKAGING DENSITIES.

Board	S/C Package	ICs/ft³
Large MLB Case		
Maximum	Flat Pack	13,221
	DIP	8,229
Typical	Flat Pack	10,733
	DIP	6,646
NAFI/SHP		
Maximum	Flat Pack	11,520
	DIP	3,840
Typical	Flat Pack	9,095
	DIP	3,200

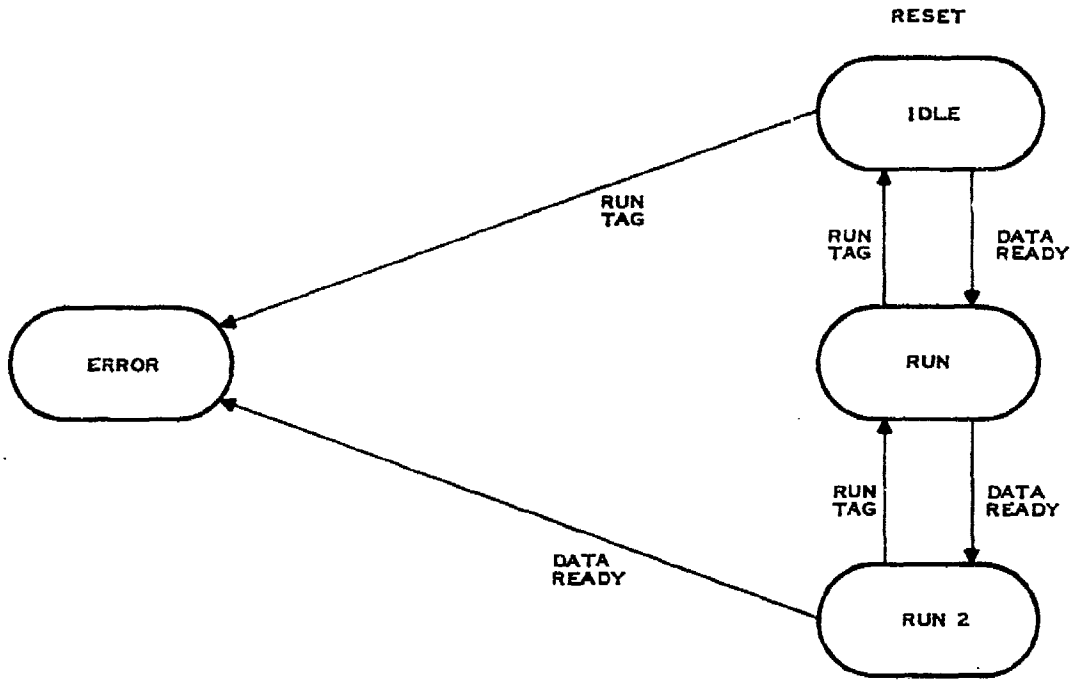


Figure 6 – Control States for Idle/Run State Controller.

board, taking into account the available board area. Typical numbers were derived, that reflected the fact that it is generally impossible to completely fill a board with integrated circuits because of system partitioning or pin limitations.

The results presented in Table 4 show that for the flat-pack ICs, the ASC and SHP packaging techniques yield comparable packaging densities. For the DIPs, the large ASC board is much more efficient. This is because considerable space is lost on the SHP board because of the DIP dimensions. Based on this brief analysis, the SHP packaging concept was adopted because of its inherent logistic advantages. The net loss in packaging density brought about by the SHP is 13 percent, which was not considered to be of first-order significance.

The definitions of various parameter limits for the SHP packaging concept were included in the packaging

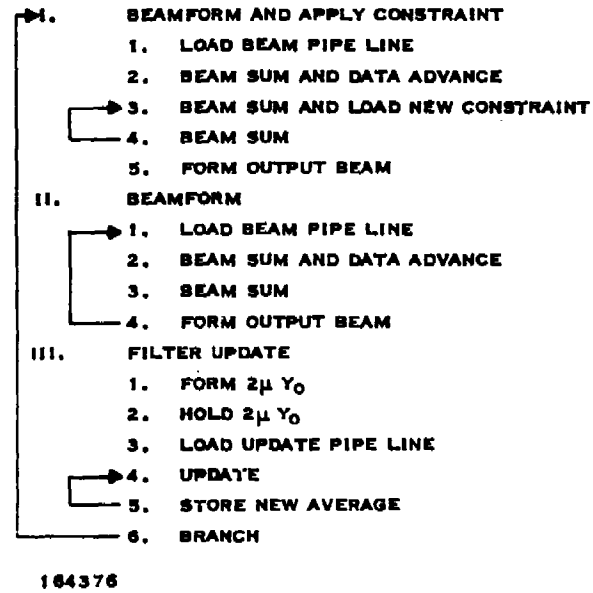


Figure 7 – Program Sequence.

technology studies conducted early in the study program. This included a study of the SHP thermal dissipation capability and a study of the available board real estate which, in turn, specifies the number of integrated circuits which may be mounted per board. In the following paragraphs, thermal analysis of the board for air-cooled and water-cooled systems are discussed; then, the various parameter limitations to include the number of integrated circuits and available pins are summarized.

2.2.4.1.1 Thermal Design for Air-Cooled Modules

The critical factor involved in the thermal design is the CCT which is defined as the component temperature beyond which reliability is adversely affected. For integrated circuits, CCT = 125°C. The temperature that the component will reach is determined by two factors, $\Delta T_{fin\text{-}to\text{-}air}$ the temperature difference between the ambient air and the module fin and $\Delta T_{device\text{-}to\text{-}fin}$, the temperature difference between the device and the fin. The temperature of the device is then given by the equation

$$\Delta T_{device\text{-}to\text{-}air} = \Delta T_{device\text{-}to\text{-}fin} + \Delta T_{fin\text{-}to\text{-}air}$$

$$\text{Temperature of Device} = \Delta T_{device\text{-}to\text{-}air} + \text{temperature of air} = \Delta T_{device\text{-}to\text{-}air+40.6°C}$$

Furthermore,

$$\Delta T_{device\text{-}to\text{-}fin} = q \times R$$

where

R = thermal resistance, device-to-fin

q = power dissipated by device.

R, the thermal resistance device-to-fin has been derived using an aluminum heatsink which is chemically milled to leave holes for the leads to get to the signal layers of the multilayer board, which is about 20 mils thick and which is put immediately below the package and cemented down with roughly a 2-mil layer of conductive epoxy. This results in a thermal resistance of about 40°C per watt from the center of the lowest device to the tip of the fin. If 0.5 watt is assumed per device, the $\Delta T_{device\text{-}to\text{-}fin}$ = (0.5 watt) (40°C/watt) = 20°C. The $\Delta T_{fin\text{-}to\text{-}air}$ has been derived for the 1A, 2A and 3A modules:

$$\Delta T_{fin\text{-}to\text{-}air} = \frac{q}{hA}$$

where

q = rate of heat transfer (Btu/hour)

h = coefficient of heat transfer fin-to-air Btu/hour ft^2 °F

A = area of dissipating surface in square feet.

The variable which is important for the 1A, 2A and 3A modules has been derived for a complex fin:

3.5 $in.^2$ for a 1A module

8.0 $in.^2$ for a 2A modules

12.5 $in.^2$ for a 3A module.

The term h is given as:

$$h = \frac{1.33\rho C_p\ V}{2(N_{pr})^{2/3}\sqrt{N_{RE}}}$$

where

ρ = density of air pounds/ft^3

C_p = specific heat of air Btu/pound °F

N_{pr} = Prandtl number

N_{RE} = Reynolds number

V = air velocity, feet/hour.

$$N_{RE} = \frac{VL\rho}{\mu}$$

where

L = length of plate in feet

μ = dynamic viscosity of air, lb/hr-ft

V, ρ = (as above).

$$h = \frac{(1.33)(0.0704)(0.240)(60{,}000)}{(2)(0.796)(133)} = 6.4 \text{ for a 1A module}$$

The various constants used are also given in Reference 2.

For a 2A module,

$$\sqrt{N_{RE}} = 206.7$$

and

$$h = \frac{(6.9)(133)}{255} = 4.2$$

For a 3A module,

$$\sqrt{N_{RE}} = \sqrt{\frac{(60{,}000)(0.0704)\ 0.718}{0.0463}} = \sqrt{65{,}300} = 255$$

and

$$h = \frac{(6.4)(133)}{207} = 3.35$$

For a 1A module,

$$\Delta T°C_{\text{fin-to-air/watt}} = \frac{q}{hA} = \frac{3.41 \text{ Btu/hour} \times 144 \text{ in}^2/\text{ft}^2}{6.4 \frac{\text{Btu}}{\text{hour ft}^2 - °\text{F}} \times 3.5 \text{ in}^2} \times \frac{5}{9} = 12.2°\text{C/watt}$$

For a 2A module,

$$\Delta T°C_{\text{fin-to-air/watt}} = \frac{3.41 \times 144}{(4.2)(8.0)} \times \frac{5}{9} = 8.1°\text{C/watt}$$

For a 3A module,

$$\Delta T°C_{\text{fin-to-air/watt}} = \frac{3.41 \times 144}{(3.35)(12.5)} \times \frac{5}{9} = 6.5°\text{C/watt}$$

For a 1A module,

$$\text{(CCT) Temp Device} = \Delta°T°C_{\text{device-to-fin}} + \text{temp air} + \Delta T°C_{\text{fin-to-air/watt}} \times \text{watts/board}$$

Power limit for a 1A board is

$$\frac{\text{(watts)}}{\text{board}} = \frac{\text{CCT} - \Delta T°C_{\text{device-to-fin}} - \text{temp air}}{\Delta T°C_{\text{fin-to-air/watt}}}$$

$$\text{Power limit for 1A board} = \frac{125°\text{C} - 20°\text{C} - 40.6°\text{C}}{12.2}$$

$$= \frac{64.4}{12.2} = 5.3 \text{ watts}$$

$$\text{Power limit for 2A board} = \frac{64.4}{8.1} = 7.95 \text{ watts}$$

$$\text{Power limit for 3A board} = \frac{64.4}{6.5} = 9.9 \text{ watts}$$

2.2.4.1.2 Thermal Design for Water-Cooled Modules

For the water-cooled case, the maximum power per board can be increased by holding the fin temperature to a constant 40.6°C. Under this condition, the temperature of the device reduces to

$$\text{Temperature of device (CCT)} = \Delta T°C_{\text{device-to-fin}} + 40.6°\text{C}$$

$$\text{Temperature of device (CCT)} = 20°\text{C} + 40.6°\text{C} = 60.6°\text{C}$$

TABLE 5 – MAXIMUM INTEGRATED CIRCUIT PACKAGE CAPACITIES OF A-SIZE SHP MODULES, ONE SIDE.

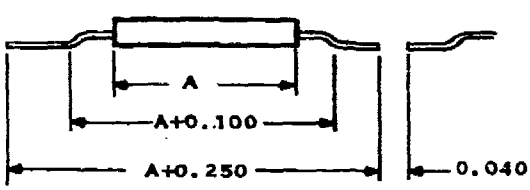
Module Size	Package Type 14-Pin W	16-Pin W	24-Pin W	14-Pin J	16-Pin J	24-Pin J
1	8	8	3	5	5	1
2	18	18	7	12	12	4
3	28	28	12	20	20	6

Module Size	Available Pins	Power (Watts) Nominal	Maximum
1	40 - [frame ground + circuit ground (0 volt) + per supply voltage]	2.25	5.3
2	80 - ["]	5.2	7.95
3	120 - ["]	8.1	9.9

The above number of packages/module is based on following:

FOR W–PACKAGE:
(FLAT PACK)

FOR J–PACKAGE:
(DUAL IN–LINE)



14 LEAD: A = 0.275
16 LEAD: A = 0.300
24 LEAD: A = 0.400

0.100 BETWEEN ADJACENT PACKAGES

for 1A, 2A and 3A modules, since $\Delta T°C_{device\text{-}to\text{-}fin}$ is constant for all three modules. As long as the power/device does not exceed 2 watts per device, the temperature of the devices shall be within the 125°C limit.

2.2.4.1.3 Summary of Packaging Limitations

Table 5 is a summary of the maximum packaging limitations for the SHP packaging technique. The limiting factors are the number of integrated circuits that can be physically mounted on the board, the maximum power dissipation that can be accommodated by the board, and the total number of pins available on the board for signal ground and power supply voltage. The numbers shown in Table 5 are based on mounting the integrated circuit packages on 40-mil spacings. For the flat pack (W package), fully extended leads are assumed as shown in Table 5. It would be possible to consider more dense packaging schemes, such as those that might be achieved, if the leads on the flat packs were trimmed or bent for insertion in plated through holes.

The parameters presented in Table 5 were used in the various tradeoff analyses conducted under this study and were used as the basis for computing the system design parameters which are discussed in succeeding paragraphs and presented in Appendix I.

2.2.4.2 System Partitioning

Initial partitioning of the system presented in Section 2.2.3 was accomplished to provide a baseline for semiconductor technology tradeoffs. Figure 8 shows schematically the partitioning accomplished on the processing element. Table 6 is a summary of the partitioned board types and data are presented relative to the number of boards used per processing element, the power dissipated by each board and a percentage of utilization of integrated circuit capacity and pin capacity. As indicated in Table 6, this partitioning was based on implementation with standard transistor-transistor logic (TTL) integrated circuits that were commercially available, with the exception of the memory board which utilizes metal oxide semiconductors (MOS) shift registers packaged in DIPs (J packs).

This particular partitioning of the processing element resulted in very efficient utilization of the board's available component capacity and its available pin capacity. In fact, the utilization figures in Table 6 show that partitioning generally tends to be either integrated-circuit or pin-limited for standard TTL. Generally, there is adequate power dissipation reserve on each of the boards.

2.2.4.3 Semiconductor Tradeoffs

The semiconductor tradeoffs investigated under this study program were limited primarily to the TTL family of intregrated circuits. MOS and ECL technologies were not considered in detail. MOS was considered to be too slow for general applicability to the ABF problem because of the extremely high throughput rates that are generally required. ECL, while being a fast circuit in terms of propagation speeds, also dissipates considerable heat. It is Texas Instruments experience that ECL requires water cooling which can be accomplished, but is not as desirable as less complicated air-cooled systems. The high-speed Schottky devices in the TTL line offer near-comparable speeds to the ECL with lower dissipation. For this reason, it was believed that investigations of high-speed Schottky devices would provide information comparable to ECL results.

2.2.4.3.1 Standard Transistor-Transistor Logic

Implementation of the Processor Element, using standard TTL logic, will take 21 boards. A summary of the module size, name, number used, power dissipation and so forth, is shown in Table 6. The PE clock period is 250 nanoseconds.

2.2.4.3.2 Available Low-Power Schottky Logic and Metal Oxide Semiconductor Memory

Implementation of the available low-power Schottky version of the Processor Element is given in Table 7. The PE has a clock period of 250 nanoseconds. The definition of "available" applies to Texaas Instruments Low Power Schottky Logic (LSTTL) integrated circuits (ICs) which are now available or are scheduled to be developed.

TABLE 6 -- STANDARD TRANSISTOR-TRANSISTOR LOGIC.

Module Name	Module Size	Number Used	Power (Watts) Used	Power (Watts) Percent of Maximum Utilized	No. Of ICs Used	No. Of ICs Percent Utilized	Pins Used	Pins Percent Utilized
4-Bit Memory Board	2A	7	4.7	54	14*	92	55	69
Constraint Memory Board No. 1	2A	1	4.5	52	14*	92	58	73
Constraint Memory Board No. 2	2A	1	5.17	59	18	100	65	82
4 x 12 Multiplier Board	2A	3	7.75	86	18	100	80	100
Multiplier Adder Tree Board No. 1	2A	1	7.33	84	17	94	77	96
Multiplier Adder Tree Board No. 2	2A	1	5.63	64	14	78	63	79
Output Board No. 1	2A	1	5.80	66	18	100	75	94
Output Board No. 2	2A	1	5.82	67	17	94	75	94
1/K Multiplier Board	1A	1	1.26	24	4	50	38	95
MOS Clock Driver Board**	2A	4	6.4	81	-	-	-	-

Mixed J and W Packages

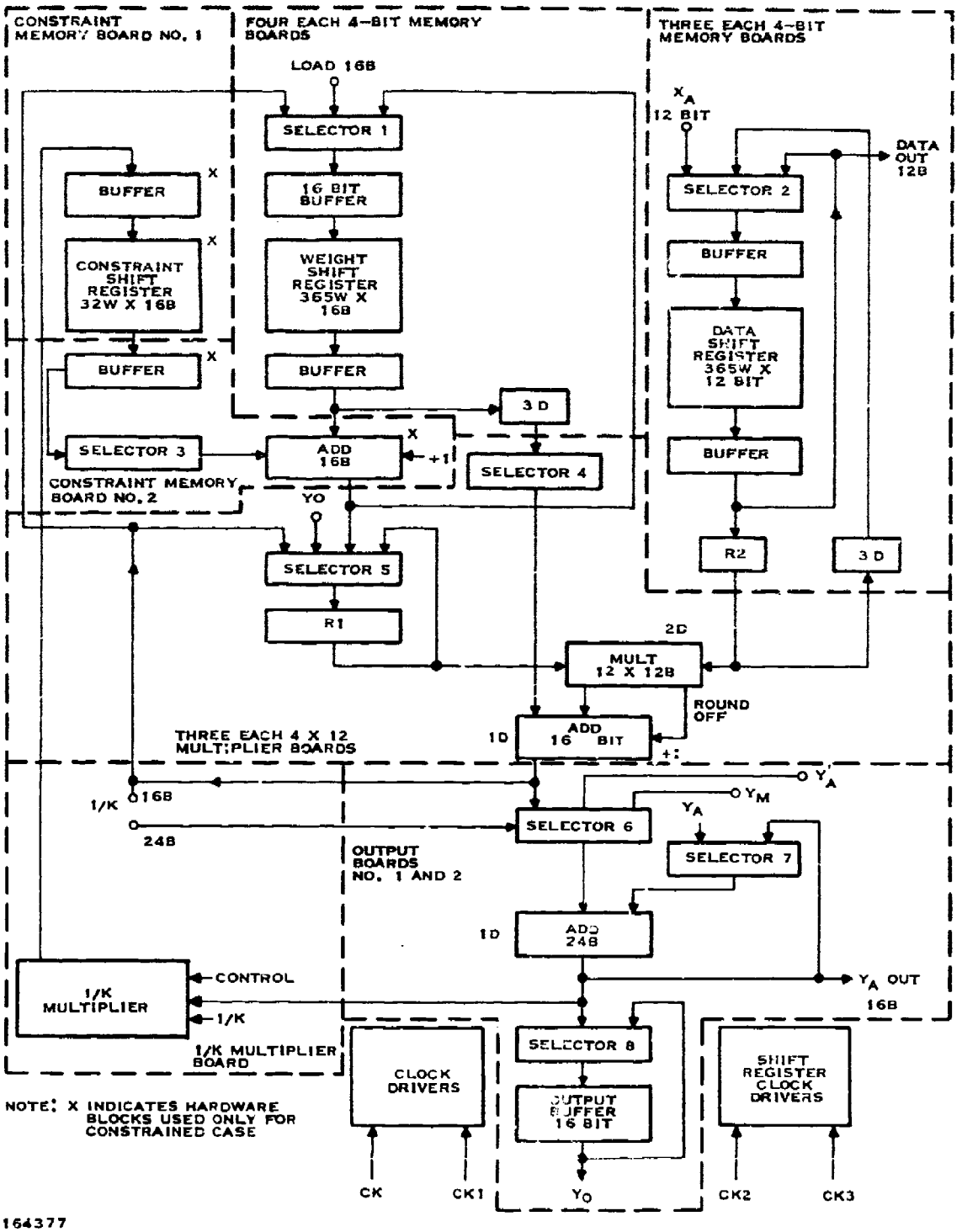


Figure 8 - Processing Element Partitioning.

TABLE 7 – AVAILABLE LOW-POWER SCHOTTKY AND MOS MEMORY.

Module Name	Module Size	No. Used	Power (Watts) Used	Power (Watts) Percent of Max Utilized	No. of ICs Used	No. of ICs Percent Utilized	Pins Used	Pins Percent Utilized
4-Bit Memory Board	2A	7	3.2	40	14*	92	55	69
Constraint Memory Board No. 1	2A	1	3.1	39	14*	92	58	73
Constraint Memory Board No. 2	2A	1	2.25	28	18	100	65	82
4 x 12 Multiplier Board	2A	3	5.03	63	18	100	80	100
Multiplier Adder Tree Board No. 1	2A	1	2.1	26	17	94	77	96
Multiplier Adder Tree Board No. 2	2A	1	1.86	23	14	78	63	79
Output Board No. 1	2A	1	1.67	21	18	100	75	94
Output Board No. 2	2A	1	1.56	20	17	94	75	94
1/K Multiplier Board	1A	1	0.340	6	4	50	38	95
MOS Closk Driver Board	2A	4	6.4	81	–	–	–	–

*Mixed J and W Packages

TABLE 8 – 100-PERCENT LOW-POWER SCHOTTKY AND MOS MEMORY.

Module Name	Module Size	No. Used	Power (Watts) Used	Power (Watts) Percent of Max Utilized	No. of ICs Used	No. of ICs Percent Utilized	Pins Used	Pins Percent Utilized
4-Bit Memory Board	2A	7	3.2	40	14*	92	55	69
Constraint Memory Board No. 1	2A	1	2.7	34	14*	92	58	73
Constraint Memory Board No. 2	2A	1	1.56	20	18	100	65	82
4 x 12 Multiplier Board	2A	3	2.1	26	18	100	80	100
Multiplier Adder Tree Board No. 1	2A	1	2.1	26	17	94	77	96
Multiplier Adder Tree Board No. 2	2A	1	1.86	23	14	78	63	79
Output Board No. 1	2A	1	1.67	21	18	100	75	94
Output Board No. 2	2A	1	1.56	20	17	94	75	94
1/K Multiplier Board	1A	1	0.340	6	4	50	38	95
MOS Clock Driver Board	2A	4	81	–	–	–	–	–

*Mixed J and W Packages

TABLE 9 – LOW-POWER, HIGH-POWER SCHOTTKY AND MOS MEMORY, 250-NS CLOCK PERIOD.

Module Name	Module Size	No. Used	Power (Watts) Used	Power (Watts) Percent of Max Utilized	No. of ICs Used	No. of ICs Percent Utilized	Pins Used	Pins Percent Utilized
4-Bit Memory Board	2A	7	3.2	40	14*	92	55	69
Constraint Memory Board No. 1	2A	1	2.7	34	14*	92	58	73
Constraint Memory Board No. 2	2A	2**	4.1	52	9	50	33	41
4 x 12 Multiplier Board	2A	6***	6.00	75	9	50	40	50
Multiplier Adder Tree Board No. 1	2A	2**	4.3	54	8 & 9	50	38	48
Multiplier Adder Tree Board No. 2	2A	1	7.95	100	14	78	63	79
Output Board No. 1	2A	1	7.72	97	18	100	75	94
Output Board No. 2	2A	1	7.53	95	17	94	75	94
1/K Multiplier Board	1A	1	0.34	6	4	50	38	95
MOS Clock Driver Board	2A	4	6.4	81	–	–	–	–

*Mixed J and W Packages

**These boards are not identical

***There are two groups of three identical boards required.

2.2.4.3.3 100 Percent LSTTL

Table 8 is a summary of the PE implemented from 100 percent LSTTL. The PE clock period is 250 nanoseconds.

2.2.4.3.4 Mixture of LSTTL, HSTTL and MOS Memory

Table 9 is a summary of the Processor Element implemented with a mixture of Low-Power Schottky Logic and High-Power Schottky Logic (HSTTL) sufficient to operate the PE at a 250-nanosecond clock period with no staging. Significant in this chart is the requirement to increase the total number of modules from 21 to 26 because of the power maximum limits on the 2A module boards. This is clearly a case of poor design, since the price of eliminating a relatively smaller number of ICs used in the staging logic is the cost of increased power and volume. Notice that the increase in board count is a result of power limitations. The extra boards required will be unique and not a common design as in the case of the memory boards.

2.2.4.3.5 LSTTL, HSTTL and MOS Shift Register Memory Operating at a 200-Nanosecond Clock Period

Table 10 is a summary of this mixture. The number of boards required to implement this mixture shows an increase from 21 to 27; however, the significant factor here is that this increase can be offset to a degree by the fact that the total number of Processor Elements for a

TABLE 10 – LOW-POWER, HIGH-POWER SCHOTTKY AND MOS MEMORY, 200-NS CLOCK PERIOD.

Module	Module Size	No. Used	Power (Watts) Used	Power (Watts) Percent of Max Utilized	No. of ICs Used	No. of ICs Percent Utilized	Pins Used	Pins Percent Utilized
4-Bit Memory Board	2A	7	3.2	40	14*	92	55	69
Constraint Memory Board No. 1	2A	1	2.7	34	14*	92	58	73
Constraint Memory Board No. 2	2A	2**	4.1	52	9	50	33	41
4 x 12 Multiplier Board	2A	6***	6.23	78	9	50	40	50
Multiplier Adder Tree Board No. 1	2A	2**	5.4	68	9 & 8	47	38	48
Multiplier Adder Tree Board No. 2	2A	2**	4.2	53	7	39	37	40
Output Board No. 1	2A	1	7.72	97	18	100	75	94
Output Board No. 2	2A	1	7.53	95	17	94	75	94
1/K Multiplier Board	1A	1	0.34	6	4	50	38	95
MOS Clock Driver Board	2A	4	6.4	81	–	–	–	–

*Mixed J and W packages
**Not identical
***Two different groups of three identical boards.

given system can be reduced by a factor of 200/250 = 0.8. The limiting speed, in reality, is the MOS memory elements which will not operate a clock period less than 200 ns.

2.2.4.3.6 LSTTL, 100-Percent HSTTL and a 256-Bit Bipolar Random Access Memory

It is assumed for the analysis below that the addressing of the bipolar Random Access Memory (RAM) is generated in the central control section of the ABF system.

Table 11 is a summary of this analysis. The significant factor in this analysis is the ability to theoretically clock the system at clock periods less than 200 ns. It should be emphasized that for the bipolar RAM, clock periods of less than 200 ns are considered technically risky; however, the results have been included for completeness of the study.

2.2.4.3.7 100 Percent HSTTL and a 1,024-bit RAM

Table 12 shows the use of a 1,024-bit bipolar RAM which is not in mass production at this time; however, there is a power dissipation savings since this unit will replace two of the 256-bit bipolar RAMs. This power savings results in a reduction in the number of boards from 35 to 28 with a net volume and power savings. Addressing for this unit is assumed to reside in the central controller. It should be emphasized that clock periods less than 200 ns are considered technically risky for the bipolar RAMs.

TABLE 11 – 100-PERCENT HIGH-POWER SCHOTTKY AND A 256-BIT BIPOLAR RANDOM ACCESS MEMORY.

			Power (Watts)		No. of ICs		Pins	
Module Name	Module Size	No. Used	Used	Percent of Max Utilized	Used	Percent Utilized	Used	Percent Utilized
4- Bit Memory Board	2A	14**	4.75	62	10 & 9	55	40	50
Constraint Memory Board No. 1	2A	1	5.34	67	14*	92	58	73
Constraint Memory Board No. 2	2A	2***	4.2	53	9	50	33	41
4 × 12 Multiplier Board	2A	6†	6.23	78	9	50	40	50
Multiplier Adder Tree Board No. 1	2A	2***	5.42	68	9 & 8	47	38	48
Multiplier Adder Tree Board No. 2	2A	2***	4.2	53	7	39	37	40
Output Board No. 1	2A	2***	4.08	51	9	50	38	47
Output Board No. 2	2A	2	7.95	100	17	94	75	94
1/K Multiplier Board	1A	1	2.18	41	4	50	38	95
MOS Clock Dirver Board	2A	4	6.4	81	–	–	–	–

*Mixed J and W packages.
**There shall be two groups of seven identical memory boards
***Not identical
†There will be two groups of three identical boards.

TABLE 12 – 100-PERCENT HIGH-POWER SCHOTTKY AND A 1,024-BIT RANDOM ACCESS MEMORY.

			Power (Watts)		No. of ICs		Pins	
Module Name	Module Size	No. Used	Used	Percent of Max Utilized	Used	Percent Utilized	Used	Percent Utilized
4-Bit Memory Board	2A	7	7.0	88	14*	92	67	84
Constraint Memory Board No. 1	2A	1	5.34	67	14*	92	58	73
Constraint Memory Board No. 2	2A	2**	4.2	53	9	50	32	41
4 × 12 Multiplier Board	2A	6***	6.23	78	9	50	40	50
Multiplier Adder Tree Board No. 1	2A	2**	5.42	68	9 & 8	50	38	48
Multiplier Adder Tree Board No. 2	2A	2**	4.2	53	7	39	37	40
Output Board No. 1	2A	2**	4.08	51	9	50	37	47
Output Board No. 2	2A	1	7.95	100	17	94	75	94
1/K Multiplier Board	1A	1	2.18	41	4	50	38	95
MOS Clock Driver Board	2A	4	6.4	81	–	–	–	–

*Mixed J and W packages
**These boards are not identical
***Two different sets of three identical boards.

TABLE 13 – SEMICONDUCTOR TRADEOFF RESULTS.

Case	Logic Mix	Memory	Effective No. of Modules	Effective Power (watts)	Total Volumn (in^3)	Total Weight
1	Standard TTL (250 ns)	MOS SR	21	117	421.7	11.9
2	Standard TTL (200 ns)	MOS SR	16.8	98.7	341.1	9.7
3	Available LSTTL (250 ns)	MOS SR	21	75.5	390.5	10.7
4	Available LSTTL (200 ns)	MOS SR	16.8	65.5	316.2	8.7
5	LSTTL and HSTTL (250 ns)	MOS SR	26	126.7	508.4	14.2
6	LSTTL and HSTTL (200 ns)	MOS SR	21.6	108.2	424.6	11.9
7	100% HSTTL (175 ns)	256 RAM	24.5	113.4	474.6	13.2
8	100% HSTTL (150 ns)	256 RAM	21	97.2	406.8	11.3
9	100% HSTTL (175 ns)	1024 RAM	19.6	96.3	383.9	10.7
10	100% HSTTL (150 ns)	1024 RAM	16.8	82.5	329.0	9.2
11	100% LSTTL (250 ns)	MOS SR	21	65.6	383.1	10.4
12	100% LSTTL (200 ns)	MOS SR	16.8	57.6	310.3	8.5
13	100% HSTTL (200 ns)	MOS SR	22.4	130.0	453.7	12.9
14	100% LSTTL (250 ns) DS Board	MOS SR	17	65.6	319.5	8.8
15	100% HSTTL (175 ns) DS Board	1024 RAM	11.9	82.5	251.1	7.2

2.2.4.3.8 Double-Sided Boards Using LSTTL

Another partitioning alternate is the use of double-sided boards for the LSTTL version of the Processor Element. Here, the limit is not power so much as it is pins.

The number of boards required for a Processor Element using LSTTL and double-sided boards results in a net savings of four boards per Processor Element. A total of 17 boards per Processor Element is required for this alternate.

The discussions above are all related to the air-cooled case. Table 13 is a summary of all the alternates discussed above.

It should be pointed out that this study is based on only a module 2A study, using the IC limits per single side given in Table 1. These results should not preclude the possibility of using more complicated packaging schemes for laying down the ICs. For example, it might be possible to improve this partitioning by bending the flat-pack leads to increase the achievable physical density.

2.2.4.3.9 Water-Cooled Partitioning

The number of modules required for each of the cases mentioned above will be a constant of 21 for the water-cooled case. This is because the power dissipated is not a limiting factor for the water-cooled version.

2.2.4.4 System Implementation

Final selection of the system implementation chosen for use in generating the *ABF Systems Designer's Handbook* must be based on optimizing system size, weight, power, and

complexity while minimizing to some degree the technical risk involved with the approach. Consideration must be given to utilizing custom Medium Scale Integration/Large Scale Integration (MSI/LSI) circuits to minimize size and weight. After careful study of all of these parameters, the Low-Power Schottky, 250-ns clock approach was selected as the baseline approach for generating the *ABF System Designer's Handbook*. This approach was deemed to be the optimum tradeoff between system size, weight, power and complexity, and technical risk.

Consideration was given to developing custom MSIs and LSIs to reduce the network count, which would have an attendant impact on system size and weight. However, the logic contained in each of the processor elements is well-structured logic consisting of addres, multipliers, registers, and so forth, that are quite adaptable to medium- and large-scale integration. A large number of MSIs and LSIs were commercially available to use in the PE. The partitioning implementation was accomplished with approximately 77-percent medium-scale integrated circuits, 22-percent large-scale integration circuits, and only 1-percent small-scale integrated (SSI) circuits. The following definitions apply to the SSI, MSI and LSI categories.

Circuit Type	Number of Gates
Small scale integration (SSI)	1 to 10
Medium scale integration (MSI)	10 to 100
Large scale integration (LSI)	Greater than 100

The circuits used in the PE are commercially available devices so that nonrecurring costs will not be incurred in procuring these circuits. No medium-scale integrated-circuit development is worthwhile and the tradeoffs for undertaking a large-scale integrated circuit development program are not at all clear based on the relatively small projected number of future ABF systems relative to the volume of commercially available integrated circuits.

Figure 9 provides further insight into the desirability of the low-power Schottky line of TTL circuits. This figure shows gate propagation delay versus gate power dissipation. A standard means of comparing integrated circuit types is to consider the device figure of merit (FOM), which is the product of the propagation delay and power dissipation. The figure of merit for each of the devices shown in Figure 9 is indicated by the device type. The smaller the figure of merit, the more desirable the device becomes. The low-power Schottky 54LS/74LS possess FOM of 20, which is the lowest of any of the devices shown in Figure 9.

In selecting the system implementation for developing the *ABF Systems Designer's Handbook*, consideration was given to using double-sided boards. Data for the double-sided boards is presented in Table 13. Mounting components on both sides of the board represents approximately a 15-percent savings in volume and approximately a 16.6-percent savings in system weight. It was decided to base system implementation on single-sided boards. It was not believed worthwhile to incur the added complexity of system manufacture for a small savings in weight and volume.

Utilizing faster devices (250-ns clock speeds) for the ABF system such as the high-speed TTL Schottky devices can offer savings in system size and weight if the clock speed is increased substantially (Table 13). However, Texas Instruments experience indicates that this would be technically risky for the SHP packaging concept. High-power Schottky devices can be used to increase the speed of digital systems. Considerable caution must be exercised if the system is to operate properly. Generally, this consists of keeping the device-to-device leads very

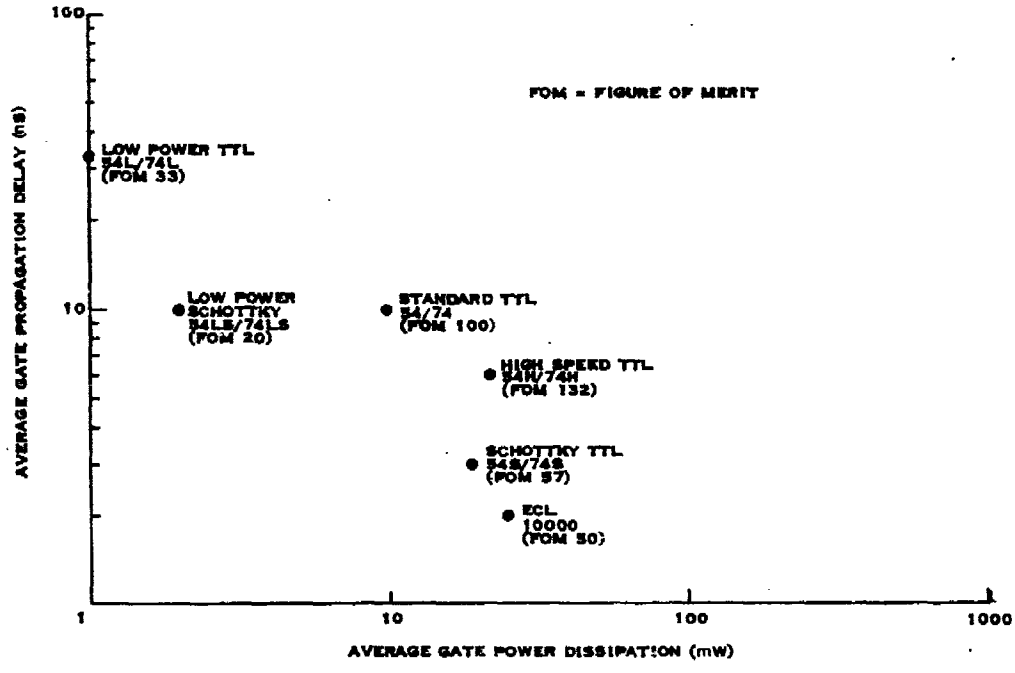


Figure 9 – Semiconductor Figure of Merit.

short (that is, less than 3 to 10 inches). The successes experienced with high-power Schottky have generally been in applications where the entire system was mounted on a single board, minimizing lead lengths. Because SHP modules are small, this approach is not feasible for the SHP packaging concept. The use of clock speeds of less than 250 ns with high-power Schottky devices is considered to be technically risky and was not considered as a viable choice for system implementation.

In summary, the low-power Schottky TTL devices appear to offer the most desirable tradeoff from the viewpoint of system size, weight, and complexity versus technical risk.

2.2.5 Handbook Generation and Module Specifications

The main objective of this study was to develop an *ABF Systems Designer's Handbook* for use by system sonar planners when making various tradeoffs relative to ABF implementation. Tradeoff factors are expressed in terms of system size, weight, power and complexity. For the purpose of this study, complexity will be measured in terms of the number of 2ASHP modules required for the system. An approach for developing equations and curves that can be easily used by the system designer was taken. This subsection describes how the basic data for these equations and curves were generated as baseline information for the *ABF Systems Designer's Handbook* which is Appendix I of this report. Appendix II of this report contains the functional module specifications generated as part of the system design and implementation study.

2.2.5.1 Size

Size is a function of the number of boards (2A SHP modules) required for the system and the amount of space required for the power supply. The number of 2A modules required for the system depends upon the number of PEs required to perform the particular ABF processing task and, in turn, the number of boards required for each PE. The number of boards per PE varies with the algorithm being performed (constrained or unconstrained) and the precision of the arithmetic calculations. The number of 2A modules required per PE as a function of algorithm and precision are:

	$P_x \times P_f$		
Algorithm	**4 × 8**	**8 × 12**	**12 × 16**
Constrained	5	11	13
Unconstrained	4	8	11

The number of PEs required for a particular processing task may be computed by the following equation:

$$\text{Number of } PE_s = \frac{N_i * N_o * F_s * L * (1 + \mu)}{4 * 10^6 * 0.9} \tag{8}$$

where

N_i = number of input channels

N_o = number of output channels

F_s = sample rate

L = filter length

μ = update rate.

The factor 0.9 represents a 90 percent processing element efficiency utilization and the factor 4×10^6 represents a clock of 250 nanoseconds.

The size of the power supply depends upon the number of processing elements and the number of memory boards utilized in the system. The number of memory boards required for the constrained and unconstrained ABF algorithms may be computed by the following equations.

$$\text{Constrained} = \frac{N_i * N_o * L}{512}\left[\frac{P_x + P_f}{4}\right] + \frac{N_o * L}{512}\,\frac{P_f}{4} \tag{9}$$

$$\text{Unconstrained} = \frac{N_i * L}{512}\,\frac{P_x}{4} + \frac{N_i * N_o * L}{512}\,\frac{P_f}{4} \tag{10}$$

The power required by the memory is computed by multiplying 4.7 watts times the number of memory boards. The power required by the processing elements (less memory) may be computed by using the following data.

	P_x/P_f		
PE (Less Memory)	12 x 16	8 x 12	4/8
Constrained	79.86	54.47	30.85
Unconstrained	73.43	52.73	26.88

These data provide basic size information in terms of the number of 2A modules and the required power for the modules in terms of dissipated power. The size may then be computed using factors developed from extensive studies of SHP packaging techniques. The factors established as reasonable guidelines are 15.9 inches^2 per 2A module and 0.75 inch^2 per watt of dissipated power.

2.2.5.2 Weight

The total number of 2A modules and the total power requirement is established; computating the other system parameters is straightforward. The factors established for computing system weight are 0.4 lb per 2A module and 0.03 lb per watt of dissipated power.

2.2.5.3 Power

Computation of the system dissipated power is explained in Paragraph 2.2.5.1 under the size calculation. To compute the total required input power by the system, only the inefficiency of the power supply need be added to the dissipated power. A 70-percent efficiency was assumed for the power supply; therefore, the total input power may be computed as (dissipated power)/0.7.

2.2.5.4 Complexity

Complexity is measured in terms of the number of 2ASHP modules contained in the system. Paragraph 2.2.5.1 describes how the total number of modules may be calculated.

2.3 Project Personnel

Personnel who have contributed to the *ABF Systems Designer's Handbook Study* are:

Name	Hours Spent on Project
James P. Edwards, III	398
John Severin	389
Ralph DuVall	458
Richard Carroll	39
A.E. Sobey, Jr.	248
L.A. Chamberlin	126
B.M. Jones	45
G.W. Neimann	81
L.L. Reagan	63
K.E. Williams	54

Mr. Emory Garth, Senior Design Engineer was responsible for the packaging concept employed in the Texas Instruments Advanced Scientific Computer (ASC), and has made a significant contribution as a consultant.

3.0 SCHEDULE

Figure 10 is an updated schedule chart that shows the project task and phasing breakdown. The task structure and phasing were somewhat modified since Reference 2 was submitted. The chart is self-explanatory.

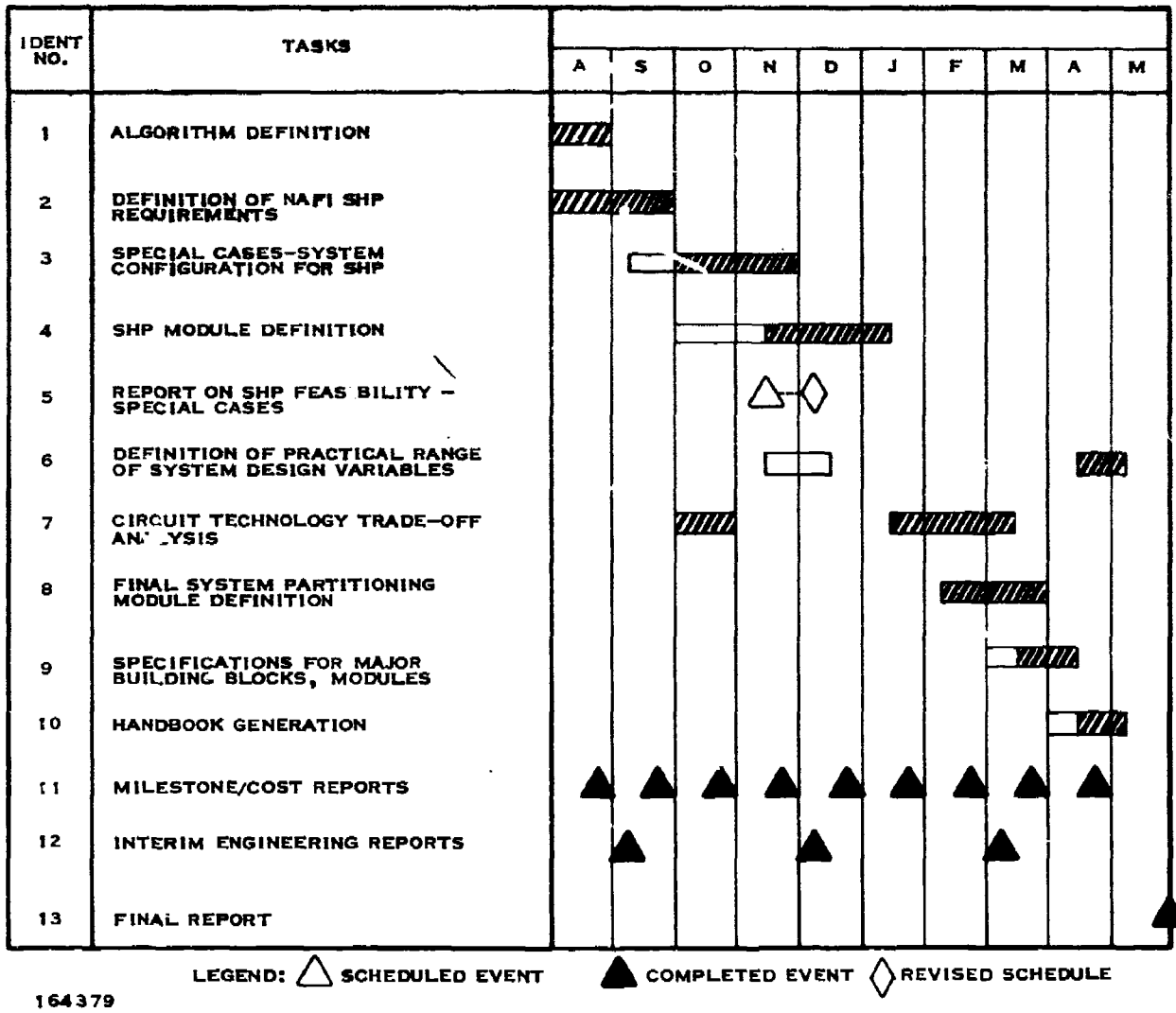


Figure 10 – Program Schedule.

4.0 CONCLUSIONS

It is feasible with presently available technology to achieve a modular and expandable approach for constrained and unconstrained filters for a large class of problems. This was achieved for all the classes of special interest defined in Section 2.2.7.3.

The following particular conclusions are made from the study.

- A high level of LSI/MSI can be achieved in the program using commercially available components.
- Module commonality for different levels of precision is not readily achievable.
- Low-power Schottky TTL technology offers the best choice for SHP packaging.
- The use of circuit boards with components mounted on both sides is not recommended for SHP packaging. This approach offers only slight improvement in size at the cost of increased production and handling complexity.
- SHP modules must be of a special class to achieve a feasible level of packaging density and suitable size.
- Custom circuit development is not cost-effective for foreseeable production levels. There would have to be other applications to make this an economical approach.
- Greatest modularity is achieved through the use of identical PEs and not through the use of identical board types within a PE.

PART II

5.0 RECOMMENDATIONS

During the course of this study, several areas that would justify additional study were discovered. However, these areas were beyond the scope of the present study and its funding. They are recommended as desirable subjects for future study. The following recommendations are made.

- Consider charge-coupled device (CCD) technology for application to the ABF. This technology offers great potential for the power-speed tradeoff and the physical size of the circuit.
- Consider a more dense circuit packing technique for SHP modules. This could be achieved by bending circuit component leads or by mounting circuit components on both sides of the board. Consideration for the SHP module tradeoff between end product reliability, ease of manufacture, and pin limitations would be required for this study. Module partitionings which minimize pin requirements would be investigated.
- Repartition the SHP modules to enhance module commonality for different precision levels. Although the goal of commonality was not achieved for all levels of precision specified for this study (4 to 16 bits), it could be achieved for some compromise levels of precision through proper partitioning.

PART III
APPENDIXES

6.0 ABF SYSTEM DESIGNER'S HANDBOOK

6.1 Introduction

The objective of this handbook is to provide the sonar system designer with design data that he can utilize in making various system-level decisions relative to adaptive beamforming (ABF) implementation. It is intended that this information be useful for backfit and new system development efforts.

Design data for tradeoff analysis is presented in the form of system size, weight, power and complexity as functions of implementation variables such as number of input channels, number of output beams, filter length, precision, and so forth. Data are presented in the form of equations for application to generalized problems, and some special cases of interest are treated with more detailed design curves, which, in addition to being useful for the special cases treated, serve as a guide to the use of basic data for generalized problems.

The designer's handbook is organized into four basic sections.

Section	Title
6.2	System Overview
6.3	ABF Design Parameters
6.4	Basic Equations
6.5	Special Cases

Section 6.2, System Overview, is designed to provide a brief summary of the ABF system design from an applications design standpoint. The design parameters required to fully specify ABF system requirements are discussed in Section 6.3. Generalized equations for arriving at system tradeoff parameters are presented in Section 6.4 Basic Equations. Finally, Section 6.5, Special Cases, presents curves showing tradeoff parameters for various special cases of interest.

6.2 System Overview

Figure 11 shows an overall block diagram for the ABF system. The system consists of multiple processing elements (PE), which are to perform beam parallel processing. Figure 11 shows PEs required to form a single output beam, Y_A. Each PE is capable of performing 4×10^6 multiply-add-add operations/second. The number of PEs required per beam depends on the computational load that is set by the choice of processing parameters discussed in the next section. The μ-PE ensembles are required for the μ-beams.

Each PE contains the necessary arithmetic and memory to perform its portion of the problem. Memory size is variable, depending on the number of input channels used to form each output beam and the input data sample rate.

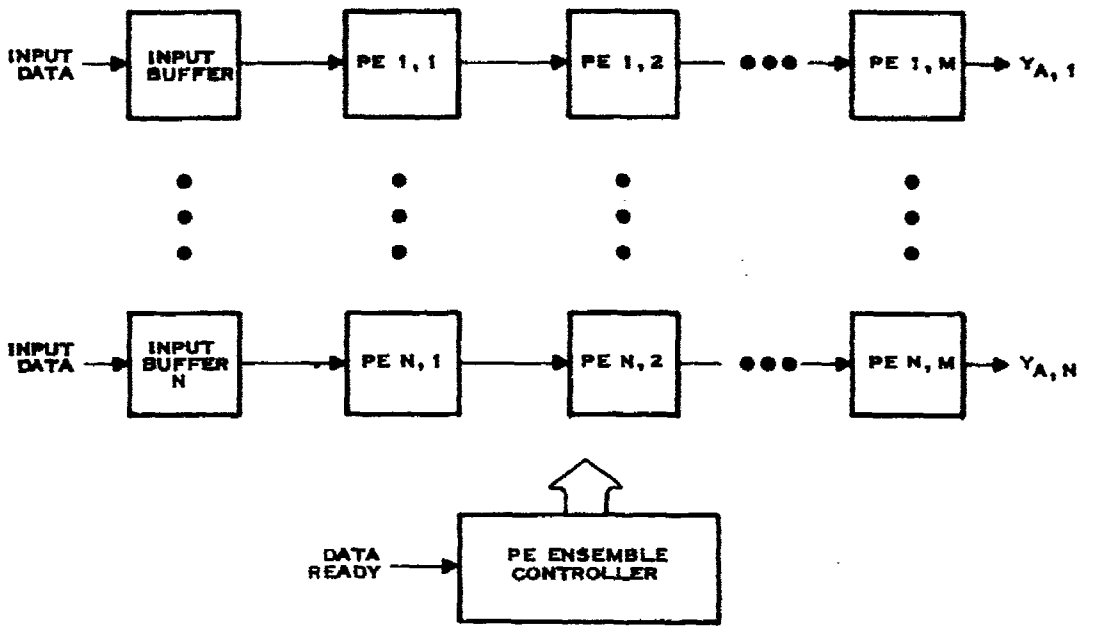


Figure 11–ABF System Overview.

Control is accomplished by a programmable PE ensemble controller (EC) which issues universal instructions to all PEs. All PEs perform the same instruction at the same time.

Input data to the system are assumed to be double-buffered. Preprocessing of the input data is assumed to be accomplished in advance of the ABF system. This might include such items as forming conventional beams for the post-adaptive beamforming applications or time delaying hydrophone channels if the ABF also provides the actual beamforming function. This approach to the interface specification was chosen to simplify the system designer's task because the handbook can then be used to estimate the amount of hardware for ABF over and above that required for conventional beamforming (CBF).

6.3 ABF Design Parameters

Design parameters required for complete ABF specification for the purpose of performing system tradeoff analysis are as follows:

a. Type of Algorithm

- Case I, Constrained: This refers to whether or not a constraint is placed on the ABF algorithm to maintain an *a priori* response to signals.
- Case II, Unconstrained.

b. Number of Input Channels (N_i)–These can be either beams, hydrophones or a combination of the two. They refer to the number of channels used per output beam.

c. Number of Output Beams (N_o)

d. Filter Length (L)--This is the number of digital sample points used to represent the filter for each channel of input data.

e. Sample Rate (F_S)--This is the per-channel sample rate of the input data.

f. Precision (P_x and P_f)--P_x is the input data precision and can be 4, 8, or 12 bits. P_f is the filter precision which can be 8, 12, or 16 bits precision. All multiplies are P_x * P_x but the full precision of P_f is used in update. Output data have a precision equal to P_f.

g. Update Rate (μ)--This is the rate at which the adaptation loop is performed.

6.4 Basic Equations

The objective of this section is to present the basic equations that may be used in developing system size, weight, power and complexity estimates.

6.4.1 Complexity

Complexity is measured in terms of the number of 2A SHP modules. This is computed as follows:

$$\text{Complexity} = (\text{number logic boards}) + (\text{number memory boards})$$

where

$$\text{Number logic boards} = (\text{number 2A modules/PE}) * (\text{Number PEs})$$

and

$$\text{Number PEs} = \left\lceil \frac{N_i * N_o * F_s * L * (1 + \mu)}{4 * 10^6 * (0.9)} \right\rceil$$

The number of 2A modules is a function of precision and the class algorithm (constrained or unconstrained) is:

	P_x/P_f		
Algorithm	**4/8**	**8/12**	**12/16**
Constrained	5	11	13
Unconstrained	4	8	12

The number of memory boards required is also a function of precision and class algorithm.

- For the constrained case

$$\text{Number of memory boards} = \frac{N_i * N_o * L}{512} \left\lceil \frac{P_x + P_f}{4} \right\rceil + \frac{N_o * L}{512} \left\lceil \frac{P_f}{4} \right\rceil \qquad (12)$$

- For the unconstrained case

$$\text{Number of memory boards} = \frac{N_i * L}{512}\left[\frac{P_x}{4}\right] + \frac{N_i * N_o * L}{512}\left[\frac{P_f}{4}\right] \qquad (13)$$

6.4.2 Power

Once complexity is computed, system input power is easily derived by

$$\text{Power} = \frac{1}{0.7}\left[(\text{Number PEs}) * (\text{Power/PE}) + (\text{Number memory boards}) * 4.7\right] \qquad (14)$$

Power is expressed in watts. Power/PE depends on the PE complexity:

	P_x/P_f		
Algorithm	**4/8**	**8/12**	**12/16**
Constrained	30.85	54.47	79.86
Unconstrained	26.88	52.73	73.43

6.4.3 Size

As with system power, size is easily derived by

$$\text{size} = (\text{complexity}) * (15.9\ \text{in}^3/\text{2A module}) + (\text{power}) * (0.75\ \text{in}^3/\text{watt}) * (0.7) \qquad (15)$$

where size is expressed in cubic inches. Complexity is the number of 2A modules in the system.

6.4.4 Weight

Weight is calculated by

$$\text{Weight} = (\text{complexity}) * (0.4\ \text{lbs/2A module}) + (\text{power}) * (0.03\ \text{lb/Watt}) * (0.7) \qquad (16)$$

Weight is expressed in pounds.

6.5 Special Cases

The following special cases of interest were defined to be given particular attention during the study.

- Case I--Constrained with three variations:

(1) $N_i = 16$; $N_c = 32$; $F_S = 5$ kHz; $L = 128$; $P_x = 12$; $P_f = 16$; $U = 1, 1/2$
(2) Same as (1) except $N_i = 32$ (17)
(3) Same as (1) except $N_i = 64$

- Case II–Unconstrained with three variations

  (1) $N_i = 1$; $N_o = 64$; $L = 128$; $F_S = 25$ kHz; $P_x = 8$; $P_f = 12$; $U = 1/64$

  (2) Same as (1) except $N_i = 2$ (18)

  (3) Same as (1) except $N_i = 4$.

These cases are treated in detail in the following paragraphs.

6.5.1 Case I–Constrained

The basic equations (Section 6.4) were solved to determine system size, weight, power and complexity as a function of input channels (N_i) for special Case I. The results are plotted in Figure 12 for both $\mu = 1$ and $\mu = ½$. The results for all parameters were linearly related to N_i with some offset at $N_i = 0$. Therefore, different scale factors can be applied to read the different parameters from the same curve as is one in the figure.

The typical case for $N_i = 64$ and $\mu = 1$, results in the following system parameters:

Size	= 272,000 cubic inches
Weight	= 7,717 pounds
Power	= 110 KW
Complexity	= 13,483 size 2A modules.

6.5.2 Case II–Unconstrained

The basic equations (Section 6.4) were solved to determine system size, weight, power and complexity as a function of input channels (N_i) for special Case II. The results are plotted in Figure 13. The results for all parameters were linearly related to N_i with no offset at $N_i = 0$. Therefore, different scale factors can be applied to read the different parameters from the same curve as is done in the figure.

The typical case for $N_i = 4$ results in the following system parameters:

Size	= 45,400 cubic inches
Weight	= 1,290 pounds
Power	= 18.7 kW
Complexity	= 2,244 size 2A modules.

7.0 MODULE FUNCTIONAL SPECIFICATIONS

Functional specifications for the modules comprising the processing element (PE) are presented in this appendix. Table 14 lists the module type and shows the number of modules required per PE.

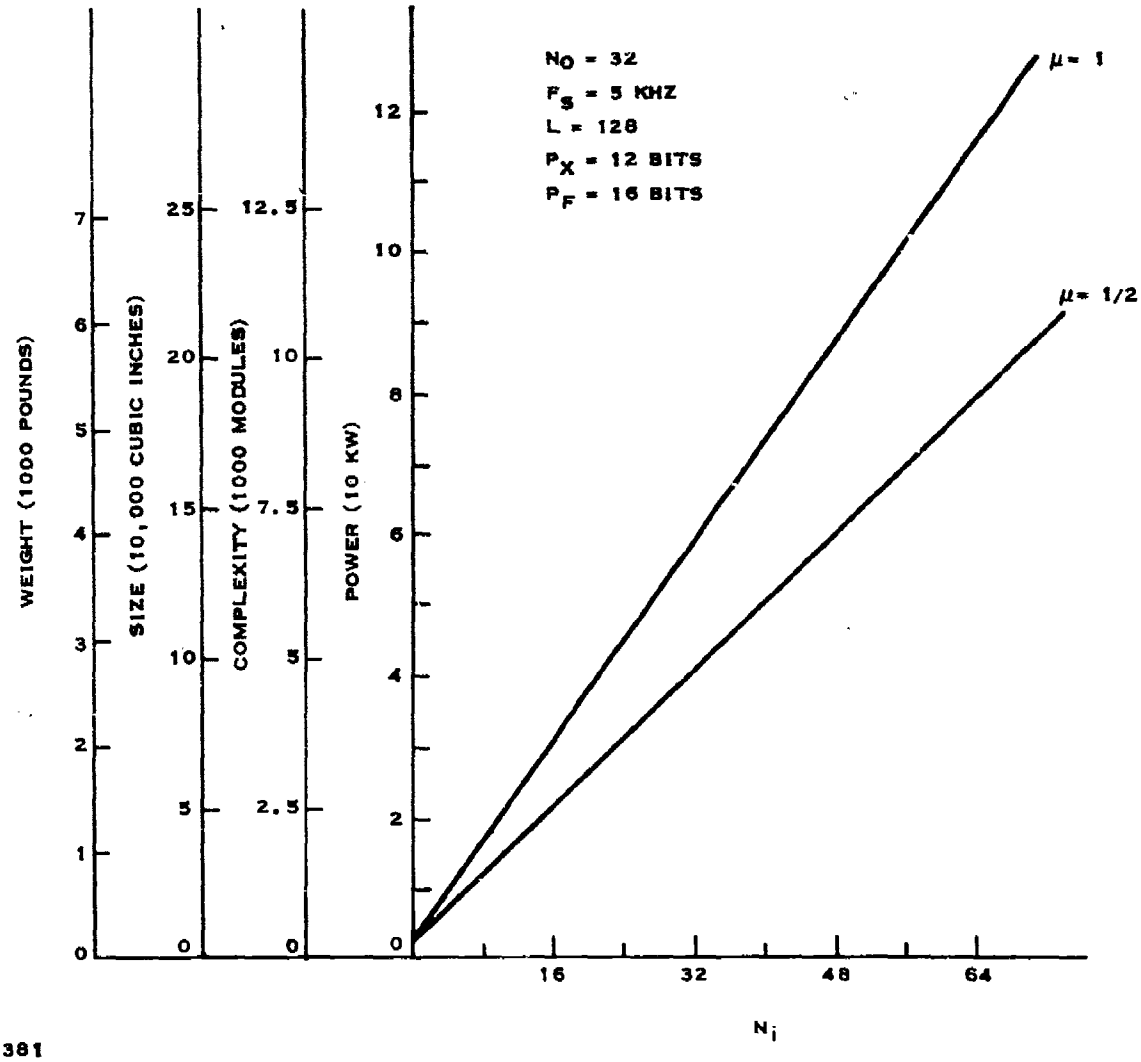


Figure 12 – Constrained Case Parameters.

TABLE 14 – LIST OF MODULE TYPES.

Name	No. Used
Adder Tree No. 1	1
Adder Tree No. 2	1
Output Board No. 1	1
Output Board No. 2	1
4 X 12 Multiplier Board	3
1/K Multiplier Board	1
4-Bit Memory Board	7–Typical
Constraint Memory Board No. 1	1
Constraint Memory Board No. 2	1

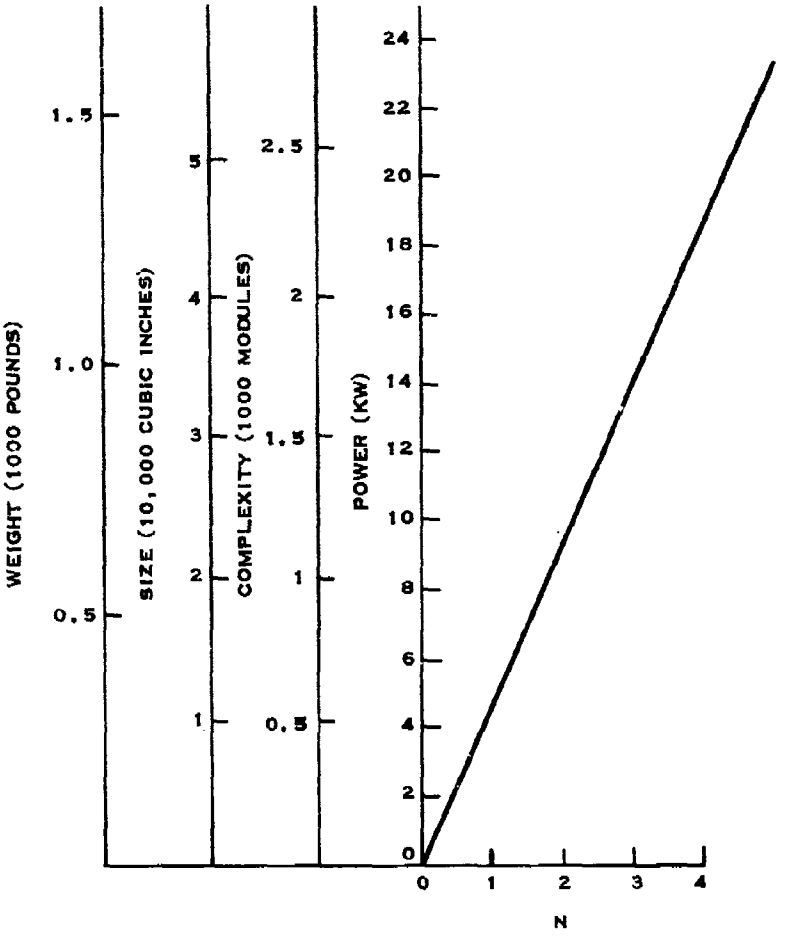


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Figure 13–Unconstrained Case Parameters

Name: Adder Tree No. 1

Special: X

Family: Digital

Repairable: No

Span: 2, Thickness: A

Functionally Specified: X

Environment: Class I

Power Dissipation: 7.33 watts

Power Requirement: +5 Vdc

FUNCTION DESCRIPTION AND DIAGRAM

This module comprises three 8-bit full adders, two 4-bit full adders, one 27-bit register, one 13-bit register and one 12-bit register interconnected to perform the adder tree function and to provide a separate delay register function. The clock inputs for the adder tree registers are tied together internally to form one common clock input. Similarly, another common clock input is formed for the delay register. One common master clear is provided for all registers.

A schematic diagram of Adder Tree No. 1 is shown in Figure 14. Parameters are given in Table 15.

TABLE 15 – ADDER TREE NO. 1.

Parameter	Minimum	Typical	Maximum	Units
Operating Frequency	0		4	MHz
Operating Temperature	0		70	°C
Input Threshold Voltage				
(a) Logic "0"	2			√
(b) Logic "1"			0.8	√
Output Voltage				
(a) Logic "0"			0.4	√
(b) Logic "1"	2.4			√
Supply Voltage	4.75	5	5.25	√
Supply Current		980		mA
Power Dissipation (50-Percent duty cycle)		4.9		Watt

The adders comprise a series of 4-bit binary full adders with full-carry look-ahead connected in cascade to extend the adder bit length to the desired length. A typical 4-bit adder diagram is shown in Figure 15.

The registers comprise a series of D-type flip-flops connected for parallel input and parallel-output operation. The number of flip-flops is extended to the desired register length. A typical 6-bit register is shown in Figure 16.

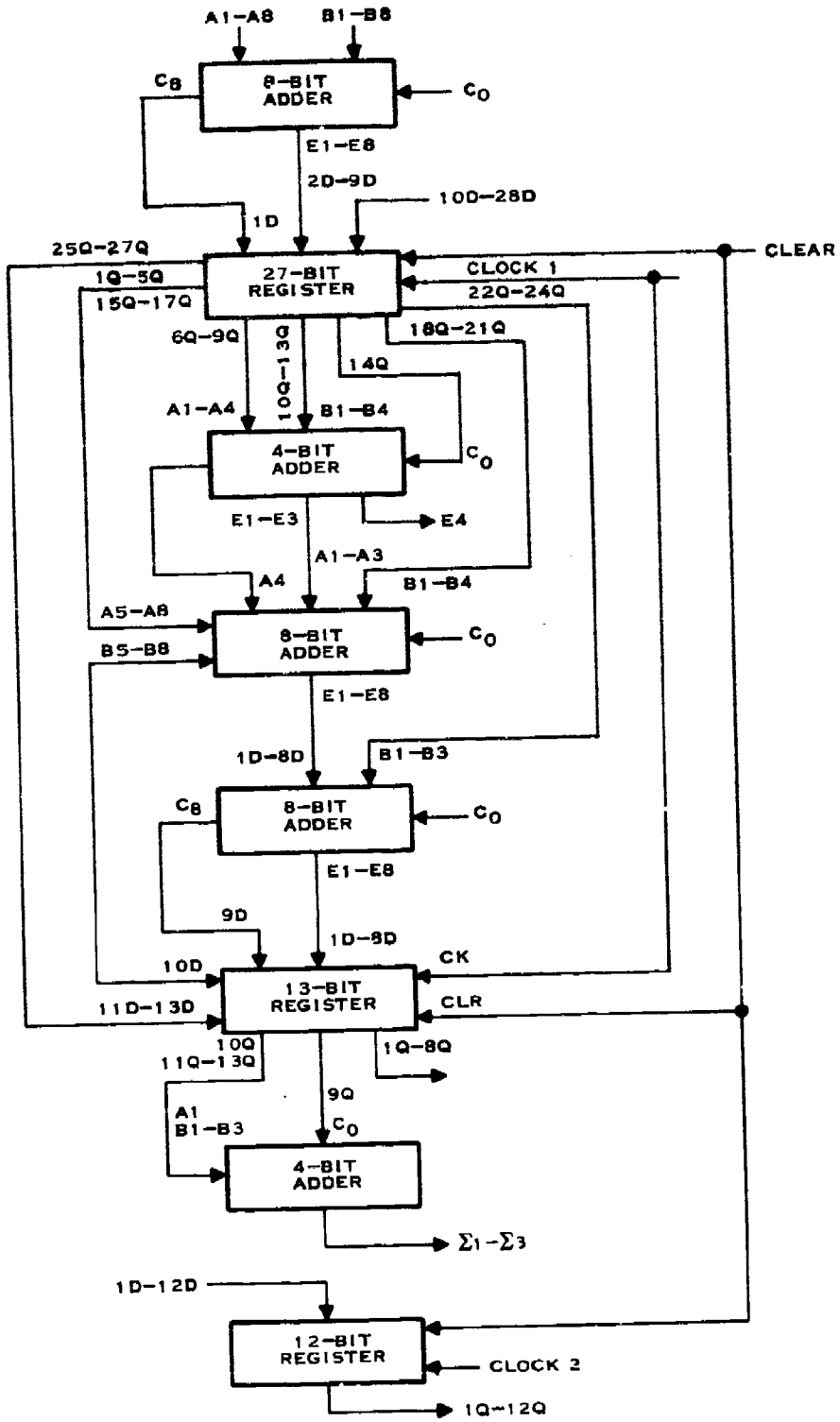

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Figure 14–Adder Tree No. 1.

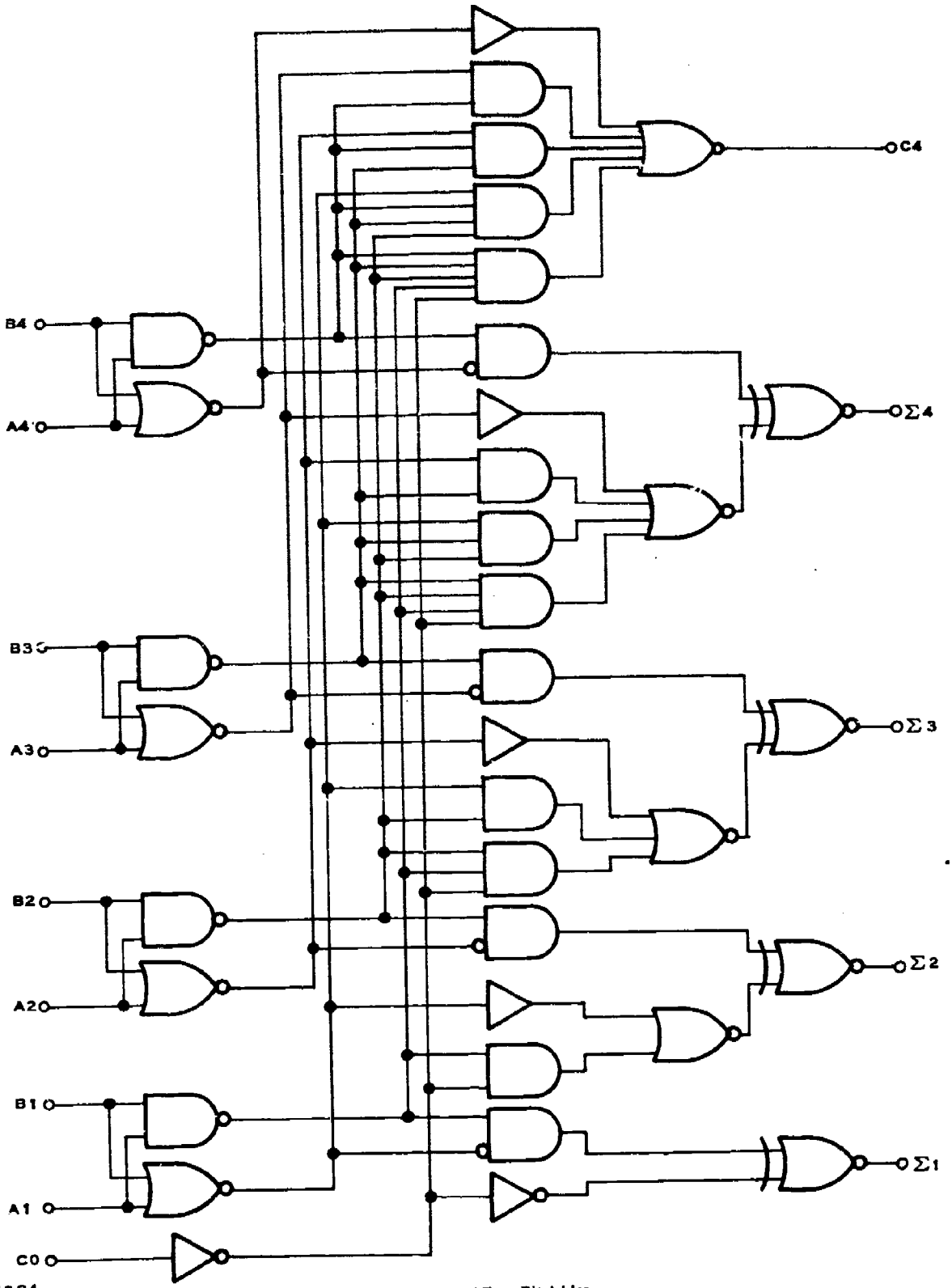

Figure 15 – Typical Four-Bit Adder.

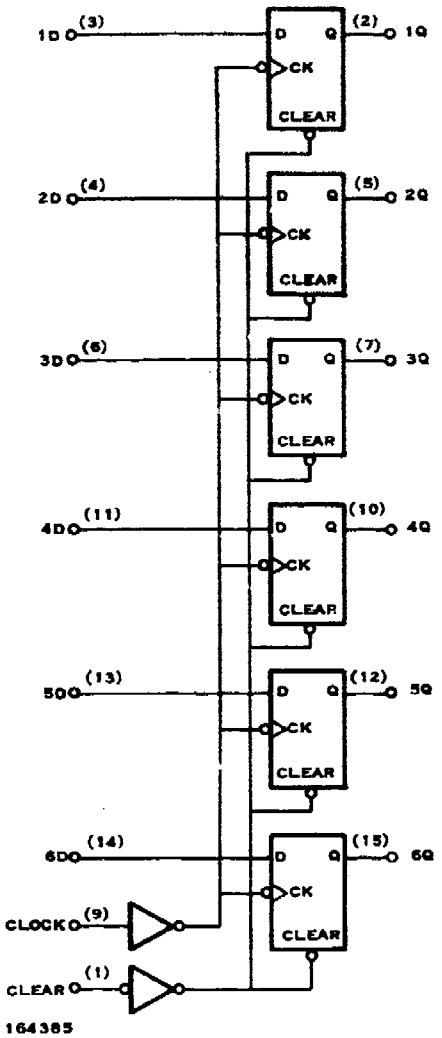

Figure 16–Typical Six-Bit Register.

Name: Adder Tree No. 2

Special: X

Family: Digital

Repairable: No

Span: 2, Thickness: A

Functionally Specified: X

Environment: Class I

Power Dissipation: 5.63 watts

Power Requirement: +5 Vdc

FUNCTION DESCRIPTION AND DIAGRAM

This module comprises two 8-bit full adders, two 4-bit full adders, one 19-bit register, one 8-bit register, one 6-bit register and one 8-bit/2-line-to-1-line data selector interconnected to perform the adder tree function and to provide a separate output-buffered data-select function.

Figure 17 is a schematic diagram of Adder Tree No. 2. Parameters are given in Table 16.

The adders comprise a series of 4-bit binary full adders with full-carry look-ahead connected in cascade to extend the adder bit length to the desired length. A typical 4-bit adder diagram is shown in Figure 18.

The registers comprise a series of D-type flip-flops connected for parallel-input and parallel-output operation. The number of flip-flops is extended to the desired register length. A typical 6-bit register is shown in Figure 19.

The 2-line-to-1-line data selector comprises a series of gates interconnected to perform the data selection function with control from both a strobe line and select line. The logic function table and diagram are given in Figure 20.

TABLE 16 – ADDER TREE NO. 2.

Parameter	Minimum	Typical	Maximum	Units
Operating Frequency	0		4	MHz
Operating Temperature	0		70	°C
Input Threshold Voltage				
(a) Logic "0"	2			V
(b) Logic "1"			0.8	V
Output Voltage				
(a) Logic "0"			0.4	V
(b) Logic "1"	2.4			V
Supply Voltage	4.75	5	5.25	V
Supply Current		760		mA
Power Dissipation (50-Percent duty cycle)		3.8		Watt

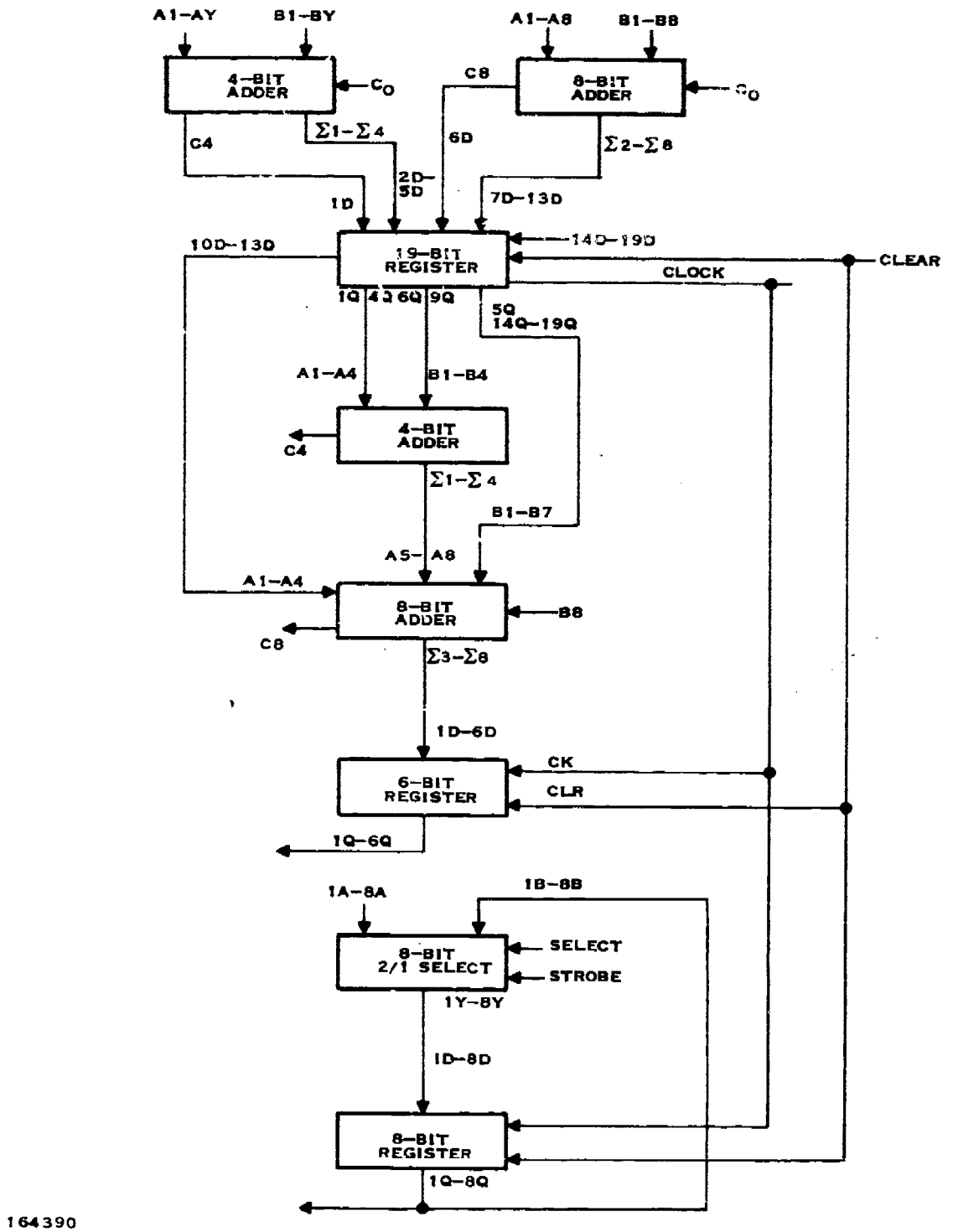

Figure 17–Adder Tree Number 2.

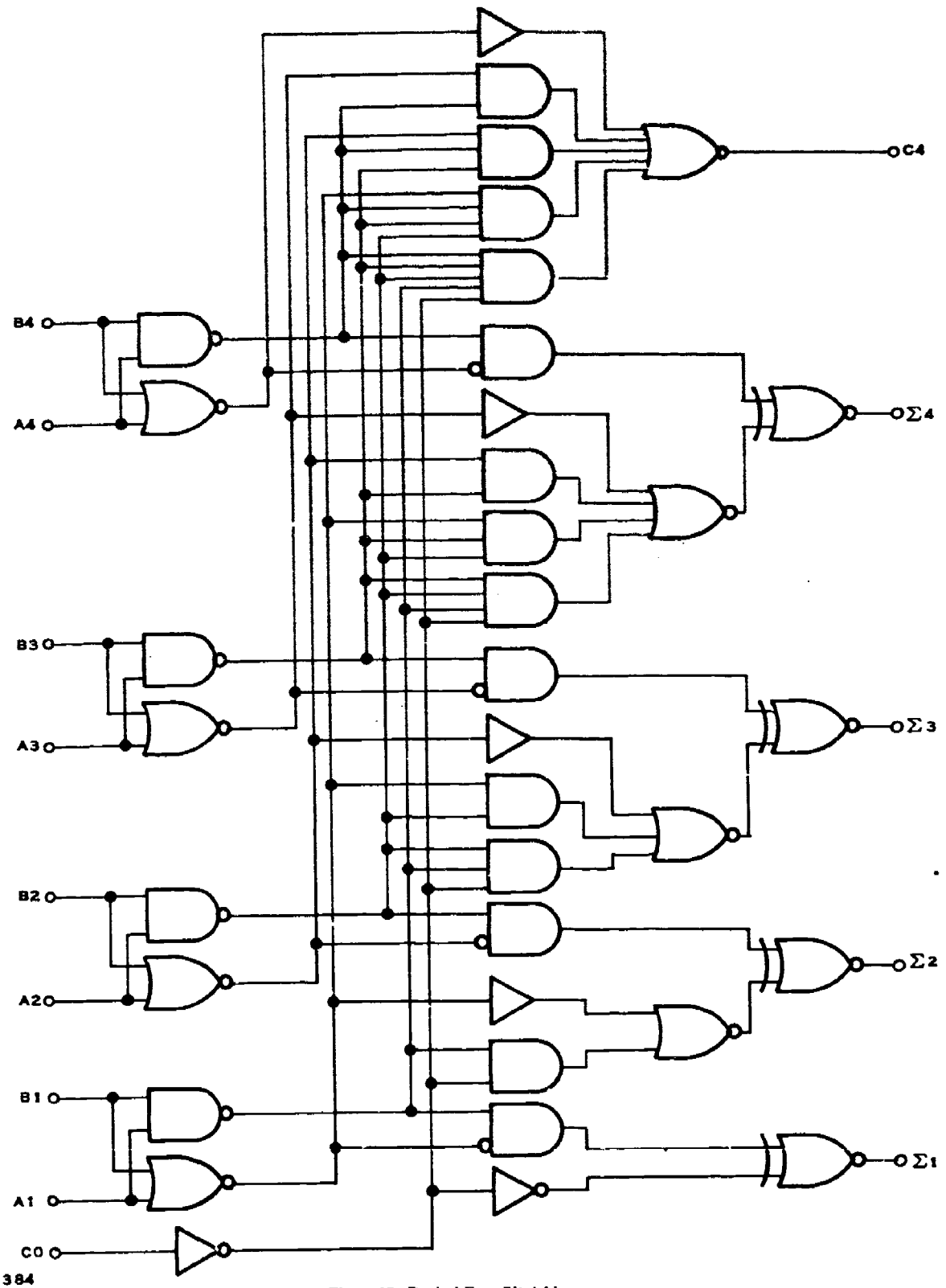

Figure 18 – Typical Four-Bit Adder.

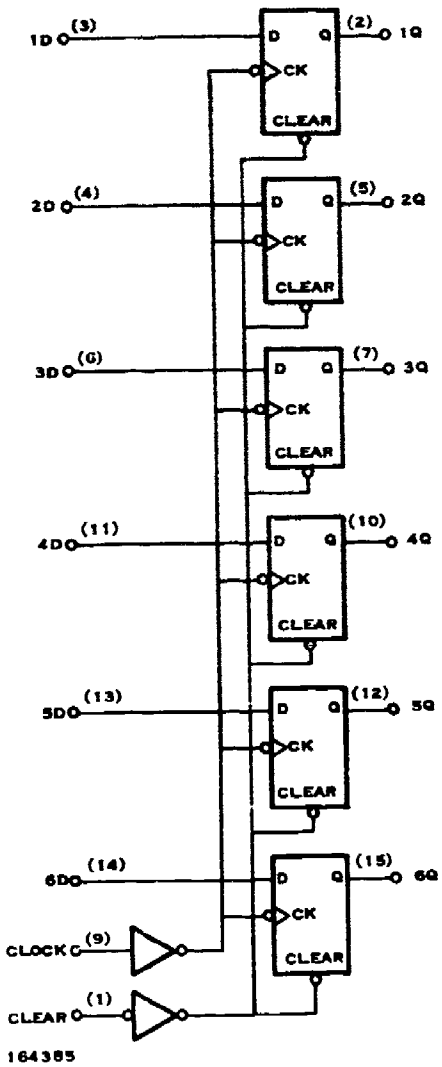

Figure 19 – Typical Six-Bit Register.

FUNCTIONAL TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH LEVEL, L = LOW LEVEL,
X = IRRELEVANT

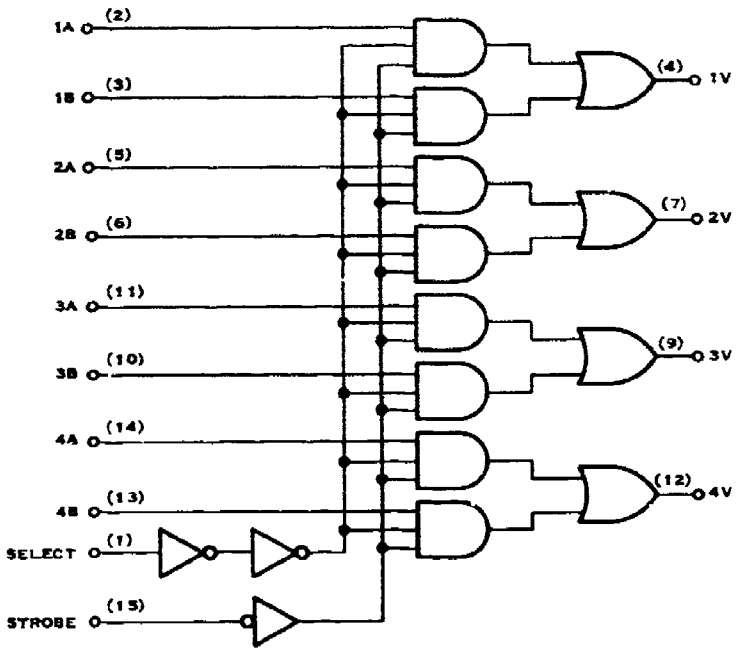

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Figure 20–Logic Function Table and Diagram.

Name: Output Board No. 1

Special: X

Family: Digital

Repairable: No

Span: 2, Thickness: A

Functionally Specified: X

Environment: Class I

Power Dissipation: 5.8 watts

Power Requirement: +5 Vdc

FUNCTION DESCRIPTION AND DIAGRAM

This module comprises one 12-bit and one 8-bit 2-line-to-1-line data selector, one 24-bit register, one 12-bit full adder, one 8-bit 4-line-to-1-line data selector and one 8-bit output register. One common clock input is provided for all the registers. Separate strobe and data-select inputs are provided for each data selector function.

Figure 21 is a schematic diagram of Output Board No. 1. Parameters are given in Table 17.

The 2-line-to-1-line data selector comprises a series of gates interconnected to perform the data selection functio· with control from both a strobe line and select line. The logic function table and diagram are in Figure 22.

The 4-line-to-1-line data selector comprises a series of gates interconnected to perform the data selection function with control from both a strobe line and select line. The logic function table and diagram are given in Figure 23.

The registers comprise a series of D-type flip-flops connected for parallel-input and parallel-output operation. The number of flip-flops is extended to the desired register length. A typical 6-bit register is shown in Figure 24.

The adders comprise a series of 4-bit binary full adders with full-carry look-ahead connected in cascade to extend the adder bit length to the desired length. A typical 4-bit adder diagram is shown in Figure 25.

TABLE 17. OUTPUT BOARD NO. 1

Parameter	Minimum	Typical	Maximum	Units
Operating Frequency	0		4	MHz
Operating Temperature	0		70	°C
Input Threshold Voltage				
Logic "0"	2			V
Logic "1"			0.8	V
Output Voltage				
Logic "0"			0.4	V
Logic "1"	2.4			V
Supply Voltage	4.75	5	5.25	V
Supply Current		760		mA
Power Dissipation (50-Percent duty cycle)		3.9		Watt

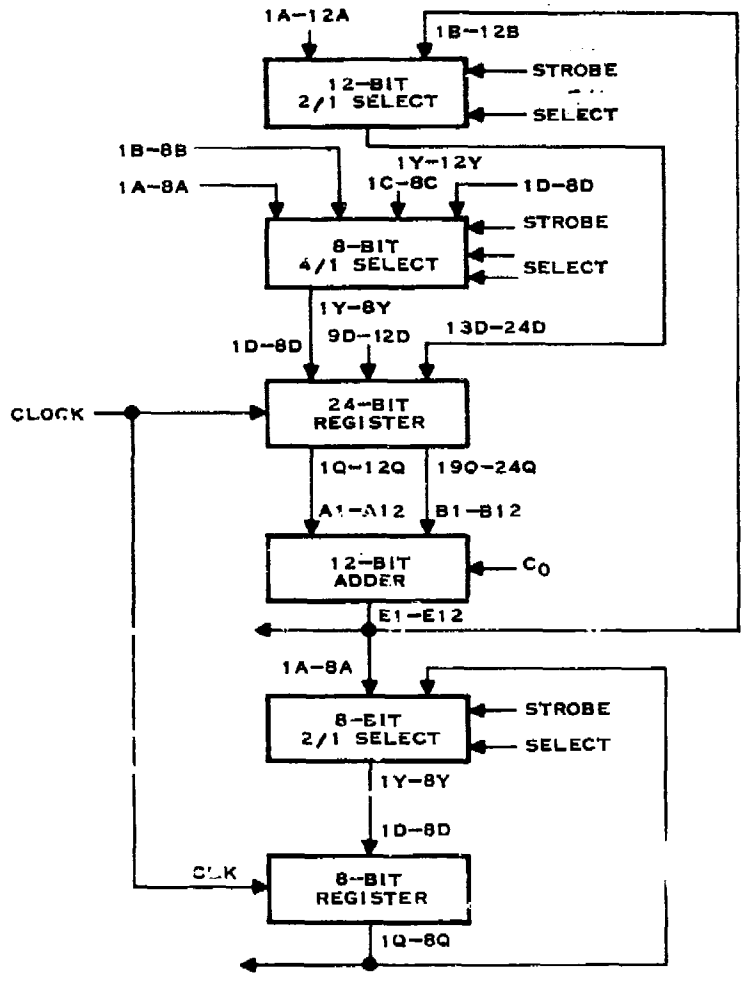

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Figure 21–Output Board Number 1.

FUNCTIONAL TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH LEVEL, L = LOW LEVEL,
X = IRRELEVANT

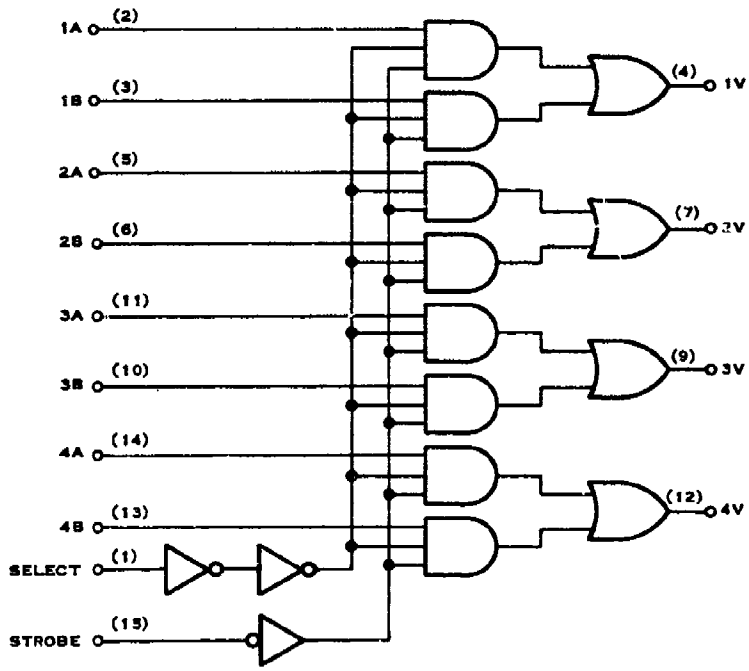

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Figure 22–Logic Function Table and Diagram.

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

SELECT INPUTS A AND B ARE COMMON TO BOTH SECTIONS

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

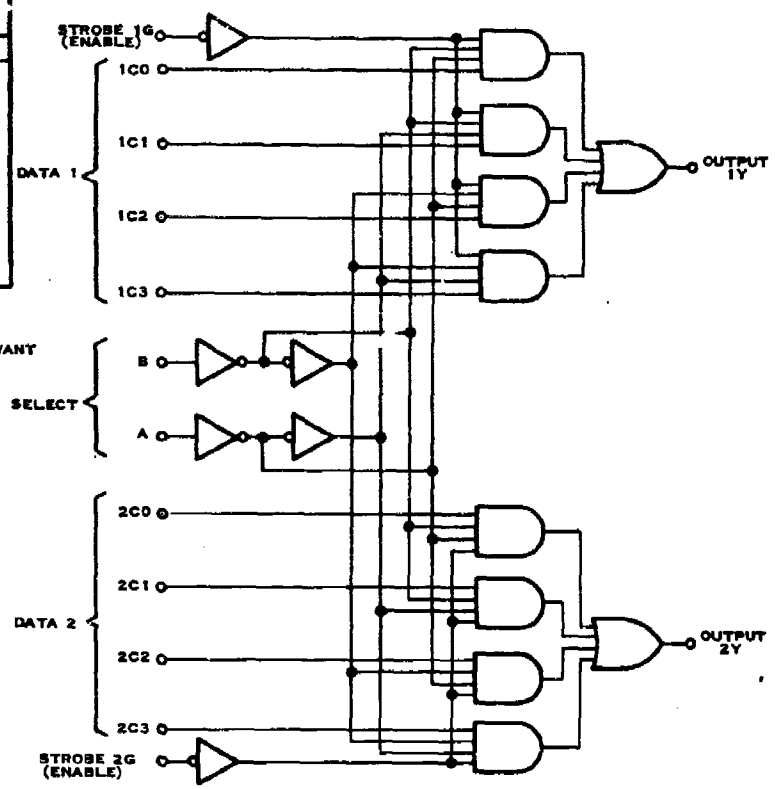

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Figure 23–Logic Function Table and Diagram.

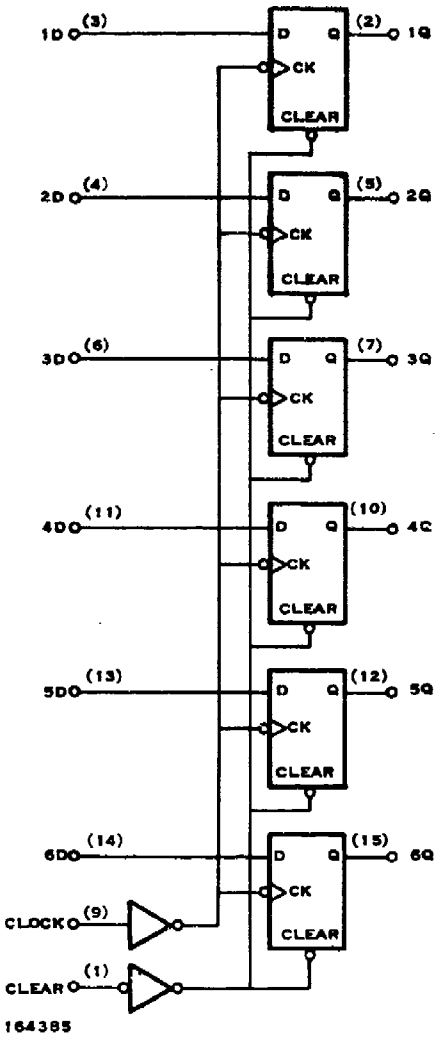

Figure 24 – Typical Six-Bit Register.

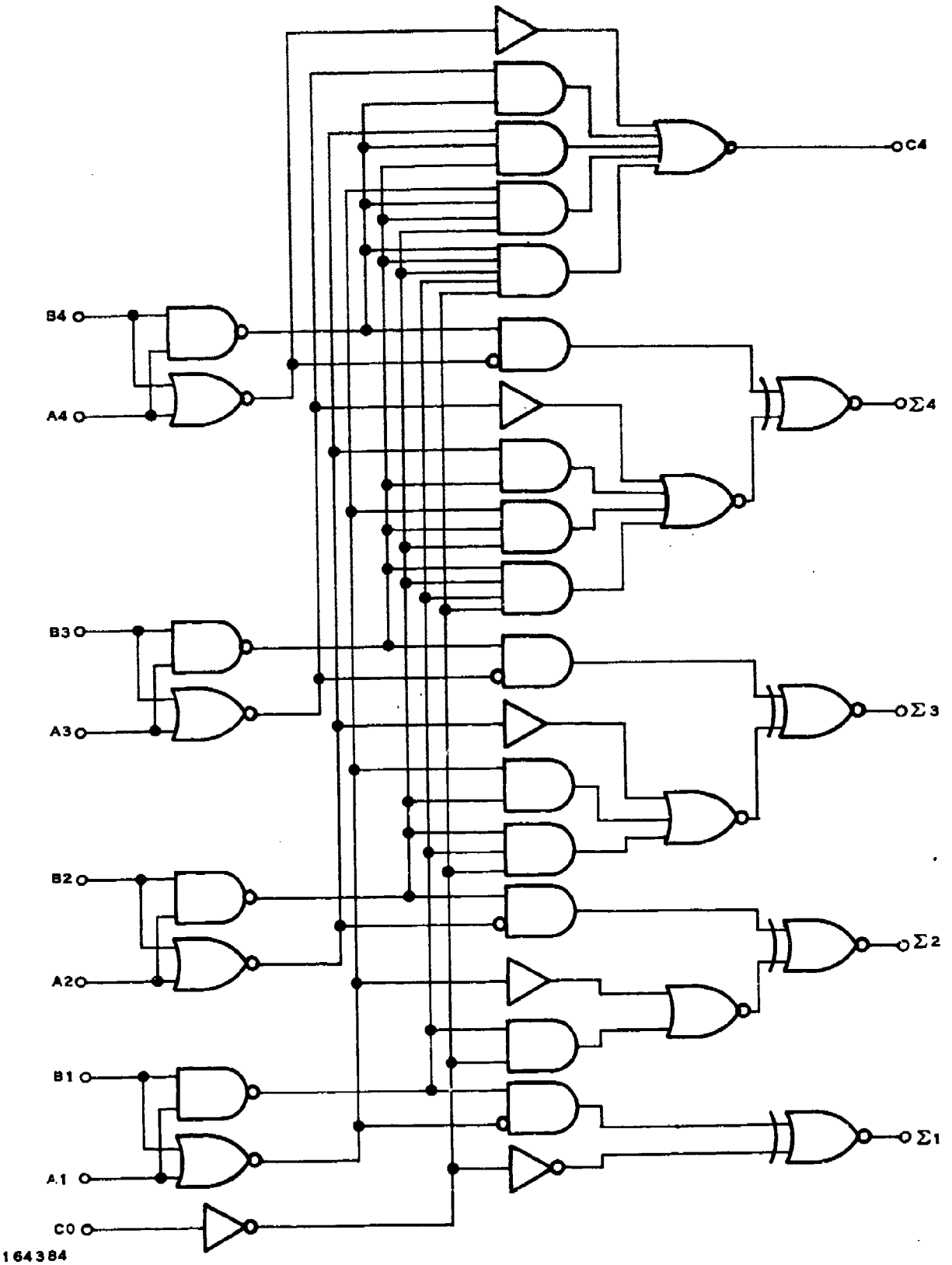

Figure 25–Typical Adder Diagram.

Name: Output Board No. 2

Special: X

Family: Digital

Repairable: No

Span: 2, Thickness: A

Functionally Specified: X

Environment: Class I

Power Dissipation: 5.82 watts

Power Requirement: +5 Vdc

FUNCTION DESCRIPTION AND DIAGRAM

This module comprises one 12-bit, one 8-bit and one 4-bit 2-line-to-1-line data selector, one 4-bit full adder, one 6-bit register, one 8-bit 4-line-to-1-line data selector, one 12-bit full adder and one 12-bit register. Separate strobe and data-select control inputs are provided for each data-selector function.

Figure 26 is a schematic diagram of output board No. 2. Parameters are given in Table 18.

The 2-line-to-1-line data selector comprises a series of gates interconnected to perform the data selection function with control from both a strobe line and select line. The logic function table and diagram are given in Figure 27.

The adders comprise a series of 4-bit binary full adders with full-carry look-ahead connected in cascade to extend the adder bit length to the desired length. Or typical 4-bit adder diagram is shown in Figure 28.

The registers comprise a series of D-type flip-flops connected for parallel-input and parallel-output operation. The number of flip-flops is extended to the desired register length. A typical 6-bit register is shown in Figure 29.

The 4-line-to-1-line data selector comprises a series of gates interconnected to perform the data selection function with control from both a strobe line and select lines. The logic function table and diagram are given in Figure 30.

TABLE 18 – OUTPUT BOARD NO. 2.

Parameter	Minimum	Typical	Maximum	Units
Operating Frequency	0		4	MHz
Operating Temperature	0		70	°C
Input Threshold Voltage				
(a) Logic "0"	2			V
(b) Logic "1"			0.8	V
Output Voltage				
(a) Logic "0"			0.4	V
(b) Logic "1"	2.4			V
Supply Voltage	4.75	5	5.25	V
Supply Current		780		mA
Power Dissipation (50-Percent duty cycle)		3.9		Watt

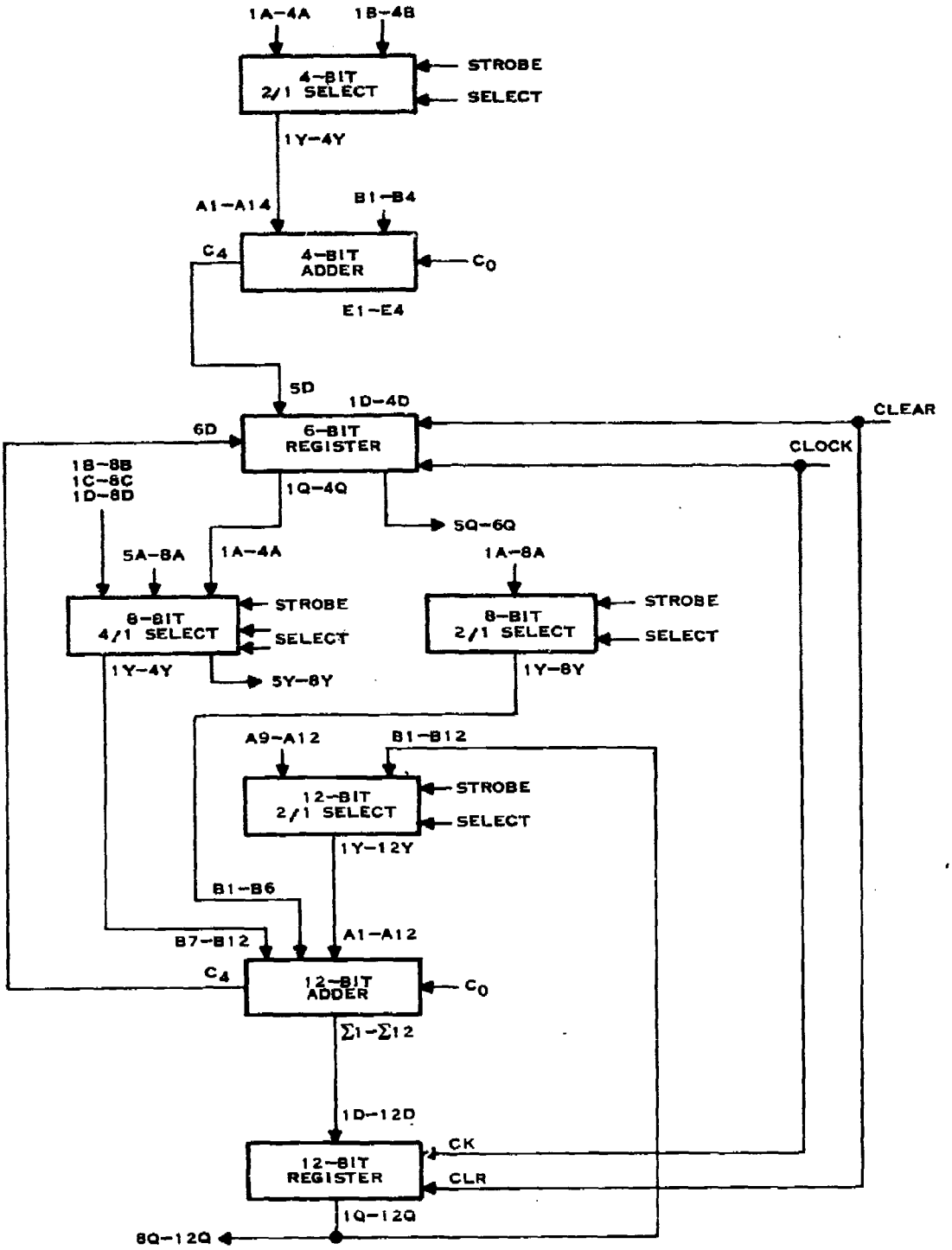

Figure 26 – Output Board Number Two.

FUNCTIONAL TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH LEVEL, L = LOW LEVEL,
X = IRRELEVANT

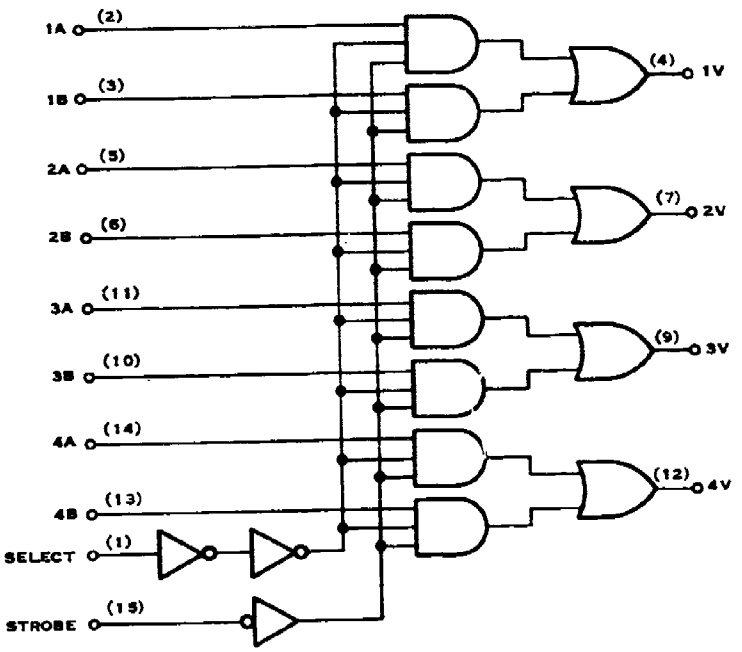

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Figure 27–Logic Function Table and Diagram.

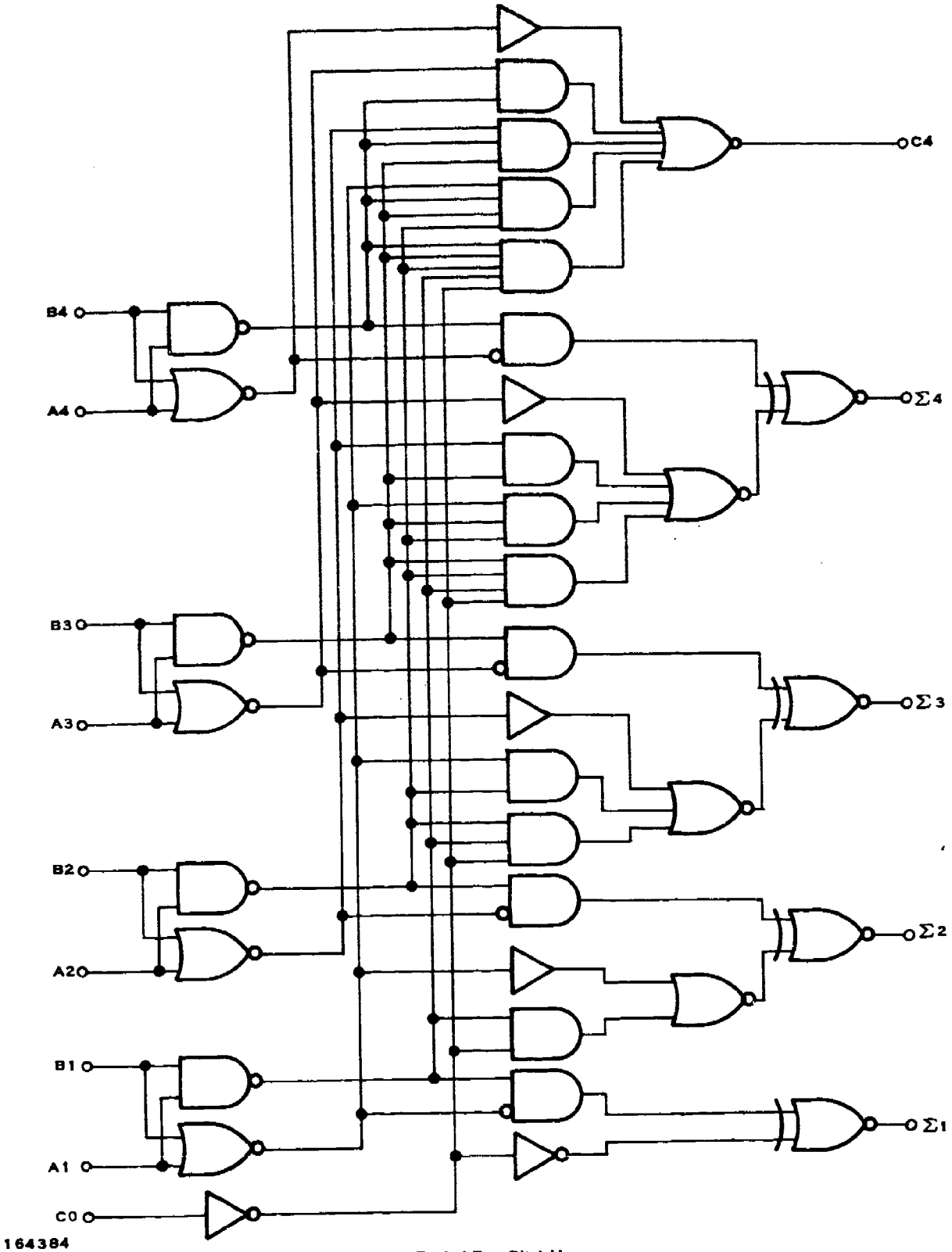

Figure 28–Typical Four-Bit Adder.

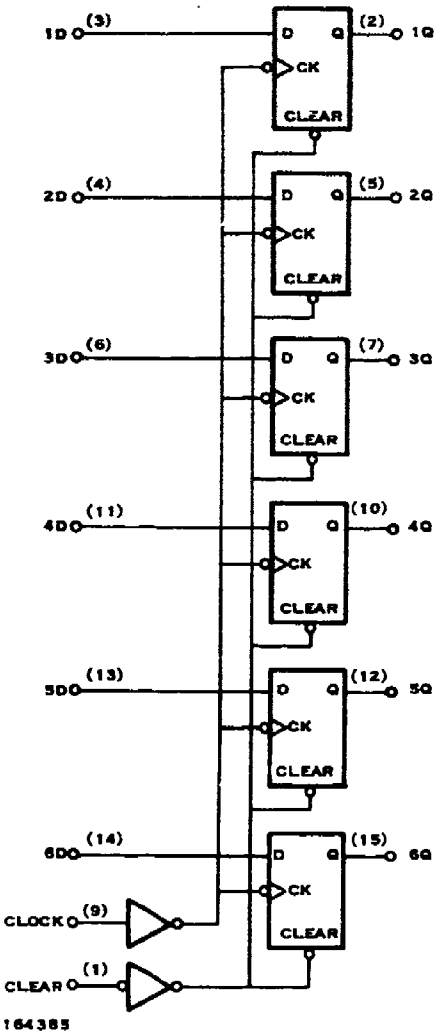

Figure 29 – Typical Six-Bit Register.

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

SELECT INPUTS A AND B ARE COMMON TO BOTH SECTIONS

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

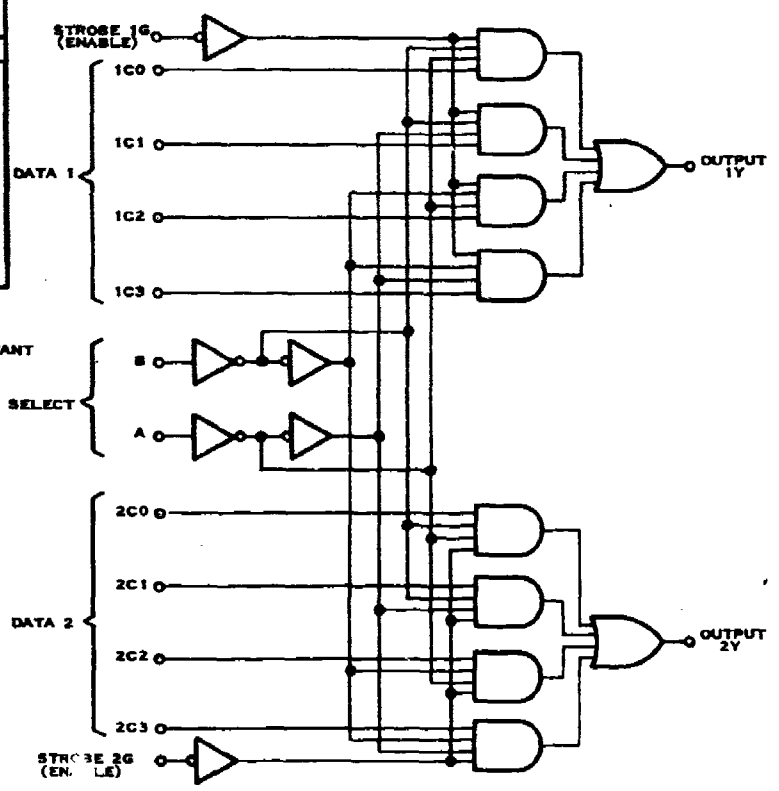

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Figure 30–Logic Function Table and Diagram.

Name: 4 X 12 Multiplier Board

Special: X

Family: Digital

Repairable: No

Spcn: 2, Thickness: A

Functionally Specified: X

Environment: Class I

Power Dissipation: 7.75 watts

Power Requirement: +5 Vdc

FUNCTION DESCRIPTION AND DIAGRAM

This module comprises one 4-bit 4-line-to-1-line data selector, four 4-bit registers, four 4 X 4 multipliers, three 4-bit 2-line-to-1-line data selectors, and three 4-bit full adders. Only data select control inputs are provided for each data selector function. The strobe inputs are omitted due to pin limitations on the module output connector.

Figure 31 is a schematic diagram of the 4 X 12 Multiplier Board. Parameters are given in Table 19.

TABLE 19 – 4 X 12 MULTIPLIER BOARD.

Parameter	Minimum	Typical	Maximum	Units
Operating Frequency	0		4	MHz
Operating Temperature	0		70	°C
Input Threshold Voltage				
(a) Logic "0"	2			V
(b) Logic "1"			0.8	V
Output Voltage				
(a) Logic "0"			0.4	V
(b) Logic "1"	2.4			V
Supply Voltage	4.75	5	5.25	V
Supply Current		1060		mA
Power Dissipation (50-Percent duty cycle)		5.3		Watt

The 4-line-to-1-line data selector comprises a series of gates interconnected to perform the data selection function with control from both a strobe line and select lines. The logic function table and diagram are given in Figure 32.

The registers comprise a series of D-type flip-flops connected for parallel-input and parallel-output operation. The number of flip-flops is extended to the desired register length. A typical 6-bit register is shown in Figure 33.

The 4 X 4 multiplier performs a binary multiplication on two 4-bit input words yielding a 8-bit product. The 8-bit product is generated with a typical delay of 40 nanoseconds or less. The provided logic function is shown in Figure 34.

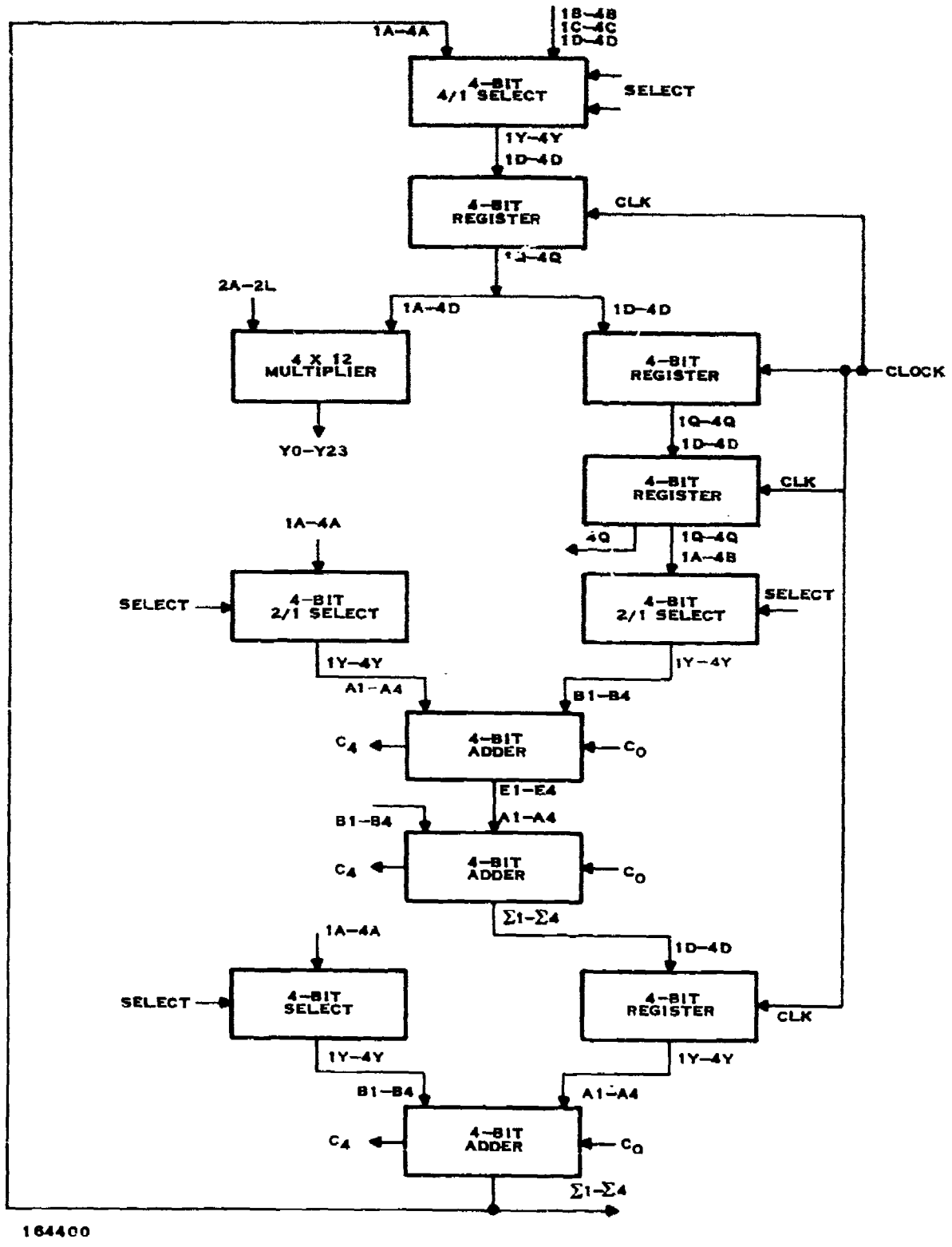

Figure 31 – Four-By-Twelve Multiplier Board.

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

SELECT INPUTS A AND B ARE COMMON TO BOTH SECTIONS

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

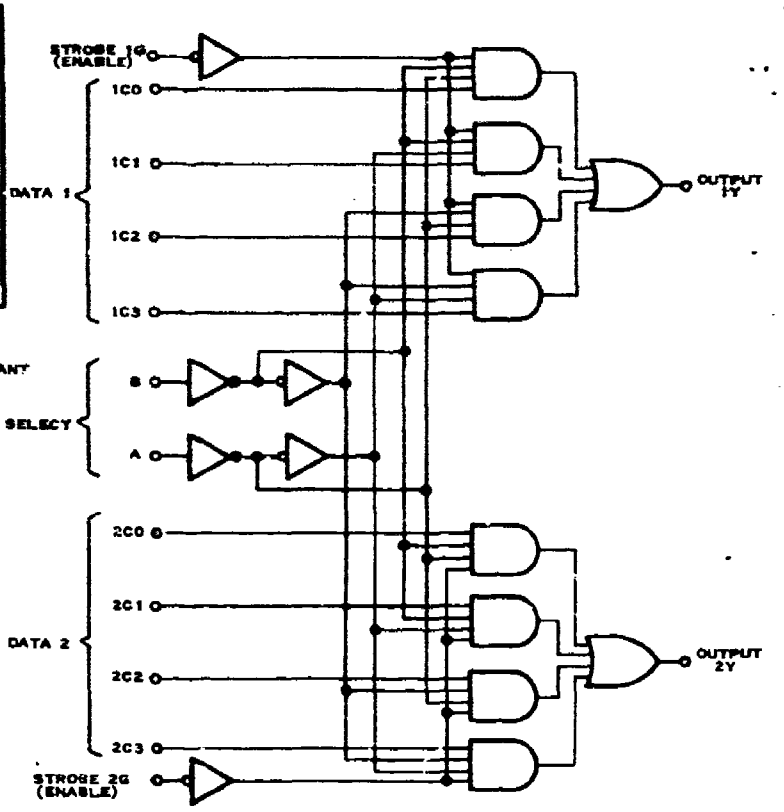

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Figure 32–Logic Function Table and Diagram.

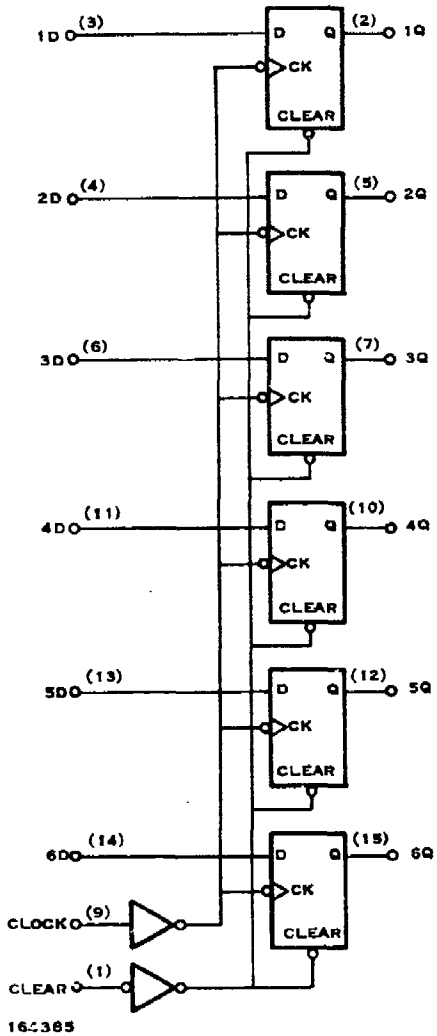

Figure 33–Typical Six-Bit Register.

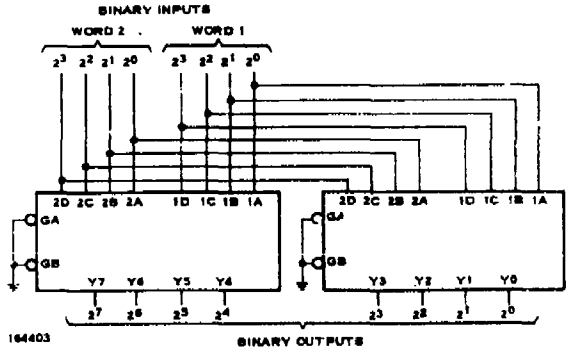

Figure 34–Four-by-Four Multiplier Logic Function.

FUNCTIONAL TABLE

INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH LEVEL, L = LOW LEVEL,
X = IRRELEVANT

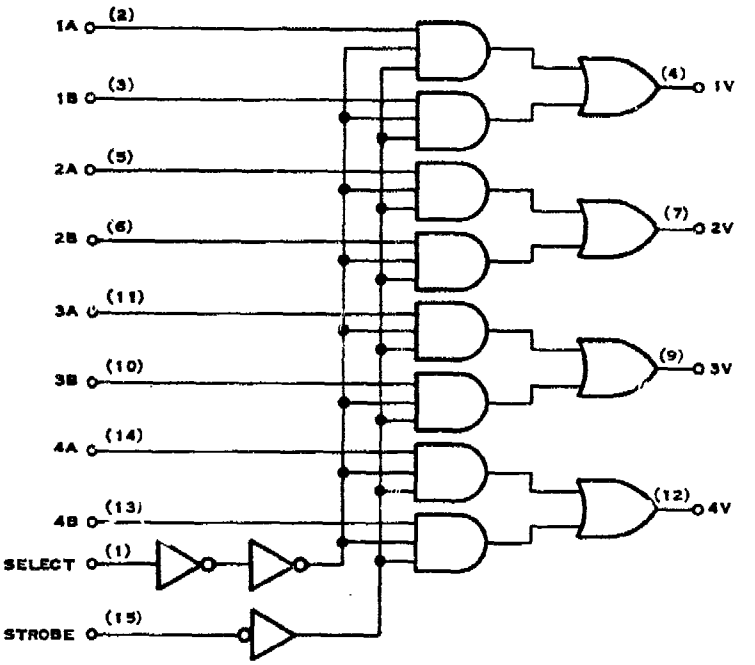

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Figure 35–Logic Function Table and Diagram.

The 2-line-to-1-line data selector comprises a series of gates interconnected to perform the data selection function with control from both a strobe line and select line. The logic function table and diagram are given in Figure 35.

The adders comprise a series of 4-bit binary full adders with full-carry look-ahead connected in cascade to extend the adder bit length to the desired length. A typical 4-bit adder diagram is shown in Figure 36.

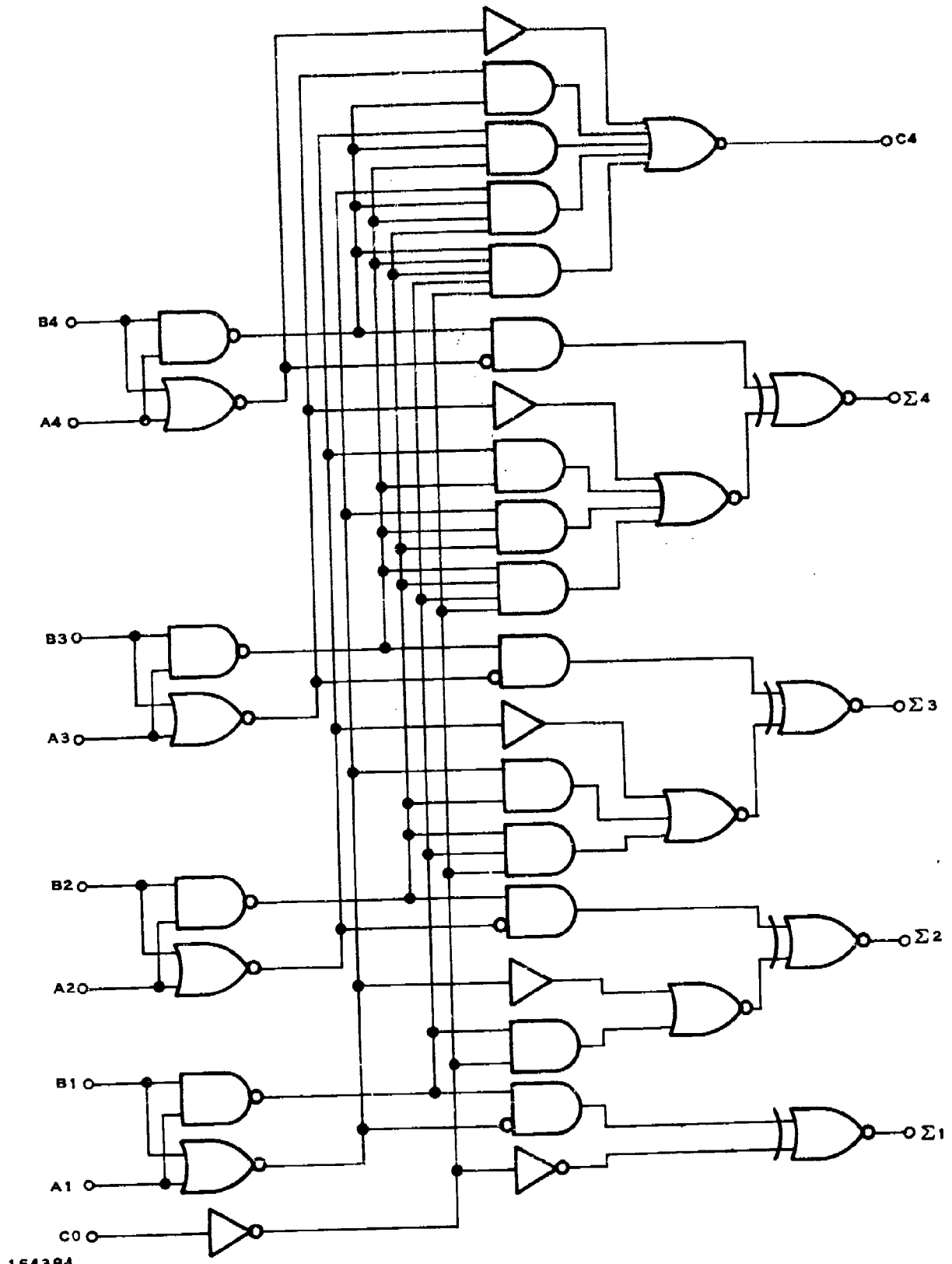

Figure 36–Typical Four-Bit Adder Diagram.

Name: 1/K Multiplier Board

Special: X

Family: Digital

Repairable: No

Span: 2, Thickness: A

Functionally Specified: X

Environment: Class I

Power Dissipation: 5.32 watts

Power Requirement: +5 Vdc

FUNCTION DESCRIPTION AND DIAGRAM

This module comprises one 16-bit shift right/parallel load register, one 16-bit 2-line-to-1-line data selector, one 16-bit full adder and one 16-bit register.

Figure 37 is a block diagram of the 1/K multiplier board. Parameters are given in Table 20.

The shift right/parallel load register comprises a series of flip-flops connected for serial shift operation or parallel load from parallel inputs operation. Parallel outputs are available for either mode of operation. The number of flip-flops is extended to the desired length. A function diagram for a typical 4-bit length is shown in Figure 38.

The 2-line-to-1-line data selector comprises a series of gates interconnected to perform the data selection function with control from both a strobe line and select line. The logic function table and diagram are given in Figure 39.

The adders comprise a series of 4-bit binary full adders with full-carry look-ahead connected in cascade to extend the adder bit length to the desired length. A typical 4-bit adder diagram is shown in Figure 40.

The registers comprise a series of D-type flip-flops connected for parallel-input and parallel-output operation. The number of flip-flops is extended to the desired register length. A typical 6-bit register is shown in Figure 41.

TABLE 20 – 1/K MULTIPLIER BOARD.

Parameter	Minimum	Typical	Maximum	Units
Operating Frequency	0		4	MHz
Operating Temperature	0		70	°C
Input Threshold Voltage				
(a) Logic "0"	2			V
(b) Logic "1"			0.8	V
Output Voltage				
(a) Logic "0"			0.4	V
(b) Logic "1"	2.4			V
Supply Voltage	4.75	5	5.25	V
Supply Current		710		mA
Power Dissipation (50-Percent duty cycle)		3.55		Watt

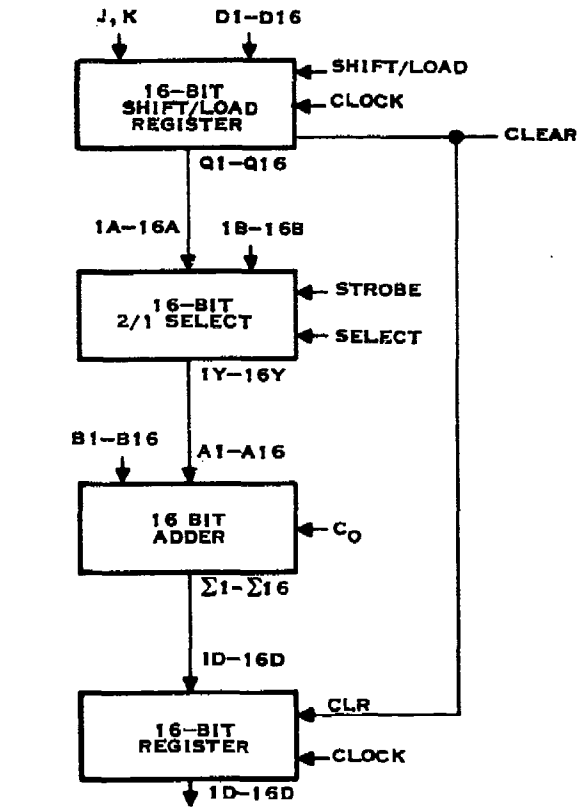

Figure 37 – 1/K Multiplier Board.

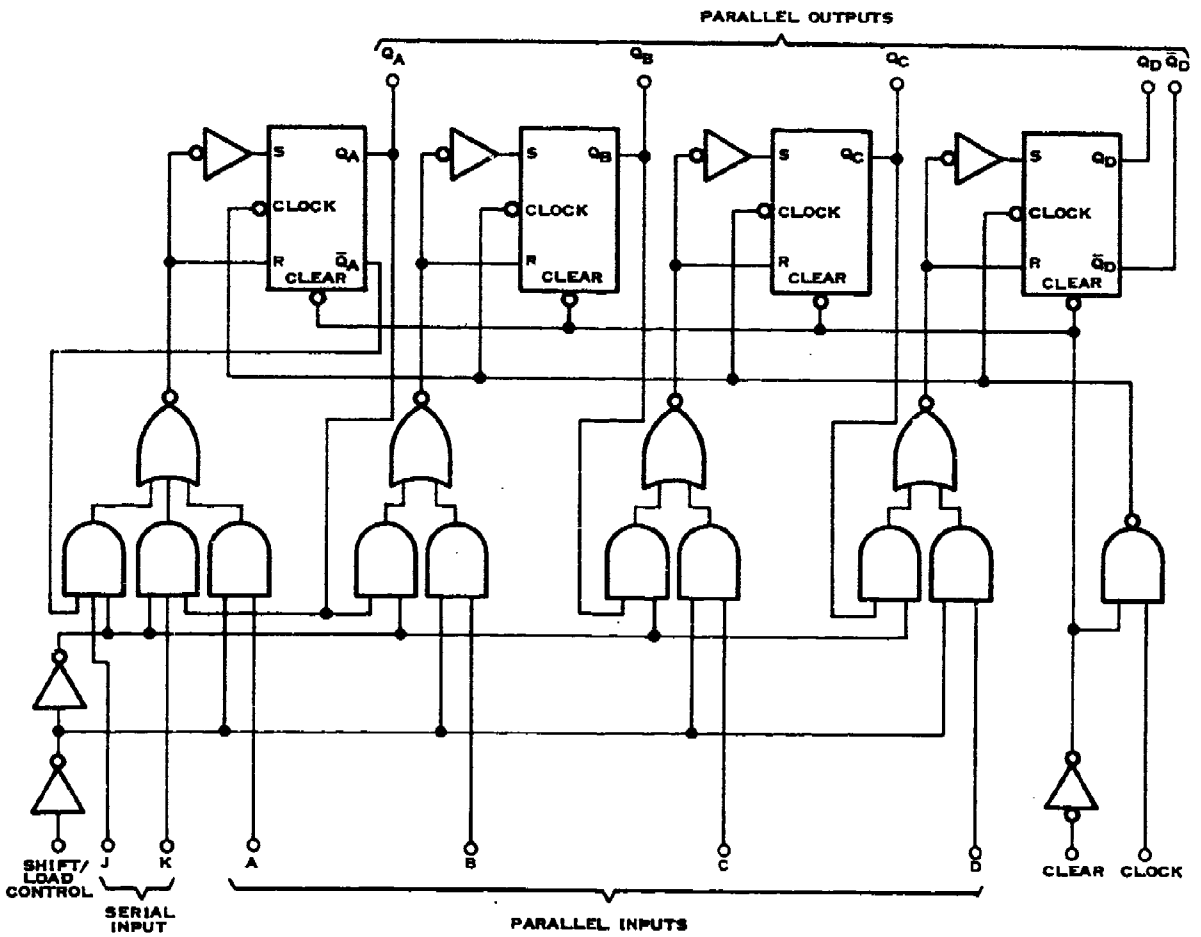

Figure 38 – Typical Four-Bit Length Functional Diagram.

FUNCTIONAL TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH LEVEL, L = LOW LEVEL,
X = IRRELEVANT

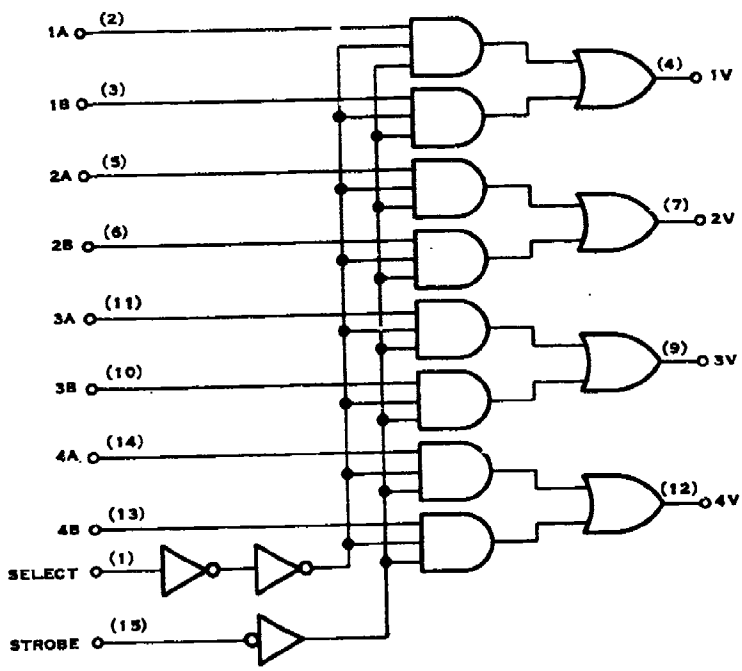

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Figure 39–Logic Function Table and Diagram.

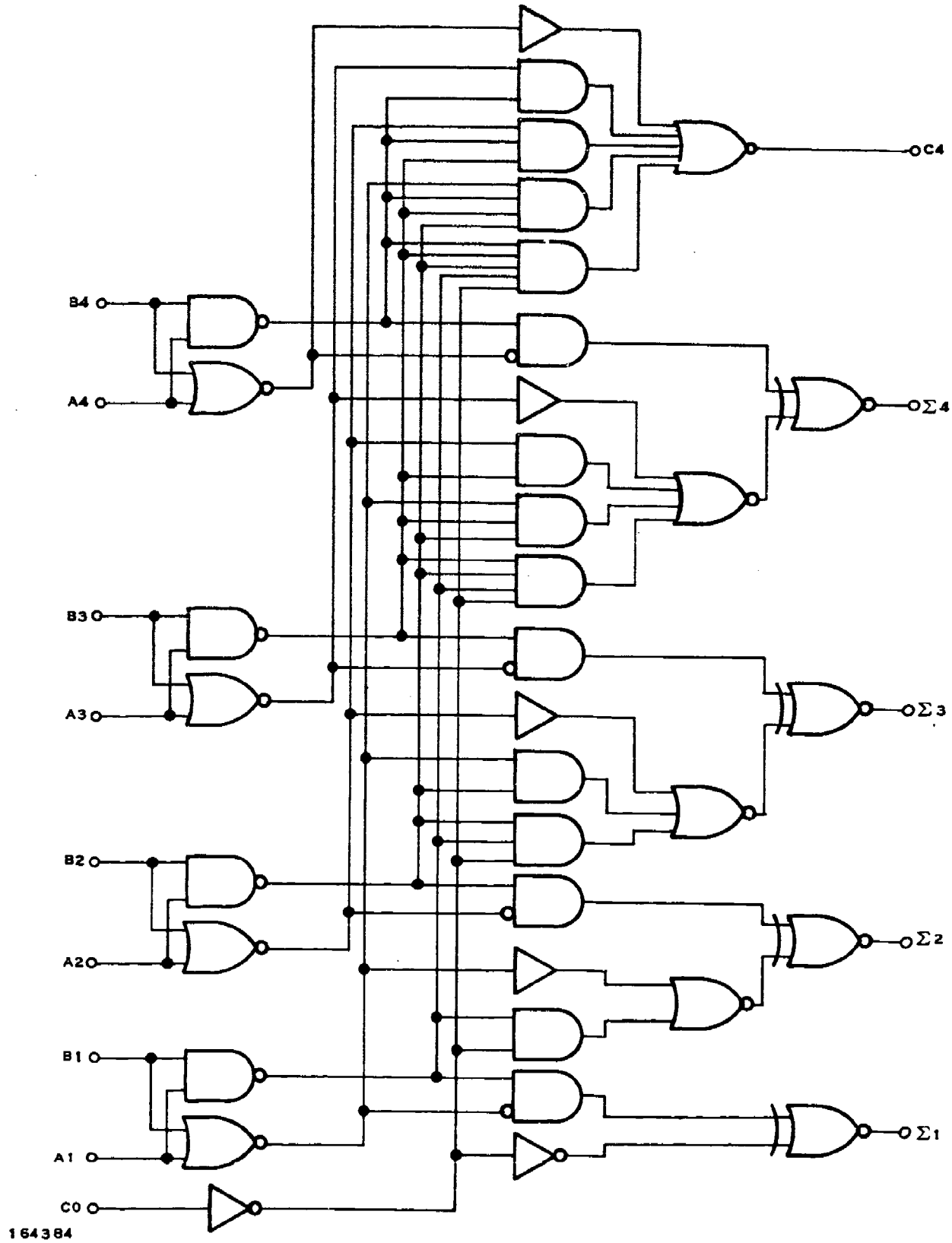

Figure 40. Typical Four-Bit Adder.

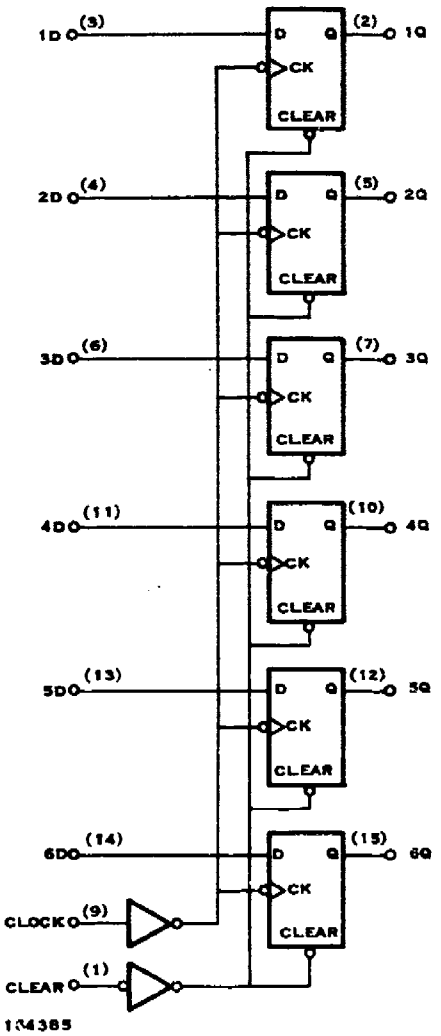

Figure 41–Typical Six-Bit Adder.

Name: 4-Bit Memory Board

Special: X

Family: Digital

Repairable: No

Span: 2, Thickness: A

Functionally Specified: X

Environment: Class I

Power Dissipation: 4.7 watts

Power Requirement: +5 Vdc

FUNCTION DESCRIPTION AND DIAGRAM

This module comprises one 4-bit 4-line-to-1-line data select, two 5-bit registers, three 4-bit registers, one parity bit generator, one parity bit checker and one 5-bit by 512-word shift-register memory. A parity bit is generated for all data entering the main memory and a parity check is made for all data leaving it. In the event of detecting a parity error, an error hold circuit is activated which holds the error indication until it is reset.

Figure 42 is a block diagram of the 4-bit memory board. Parameters are given in Table 21

TABLE 21 – 4-BIT MEMORY MODULE.

Parameter	Minimum	Typical	Maximum	Units
Operating Frequency	0		4	MHz
Operating Temperature	0		70	°C
Input Threshold Voltage				
(a) Logic "0"	2			
(b) Logic "1"			0.8	V
Output Voltage				V
(a) Logic "0"			0.4	
(b) Logic "1"	2.4			V
Supply Voltage	4.75	5	5.25	V
	−14	−12	−11	V
Supply Current		630		mA
Power Dissipation (50-Percent duty cycle)		3.15		Watt

The 4-line-to-1-line data selector comprises a series of gates interconnected to perform the data selection function with control from a strobe line and select lines. The logic function table and diagram are given in Figure 43.

The registers comprise a series of D-type flip-flops connected for parallel-input and parallel-output operation. The number of flip-flops is extended to the desired register length. A typical 6-bit register is shown in Figure 44.

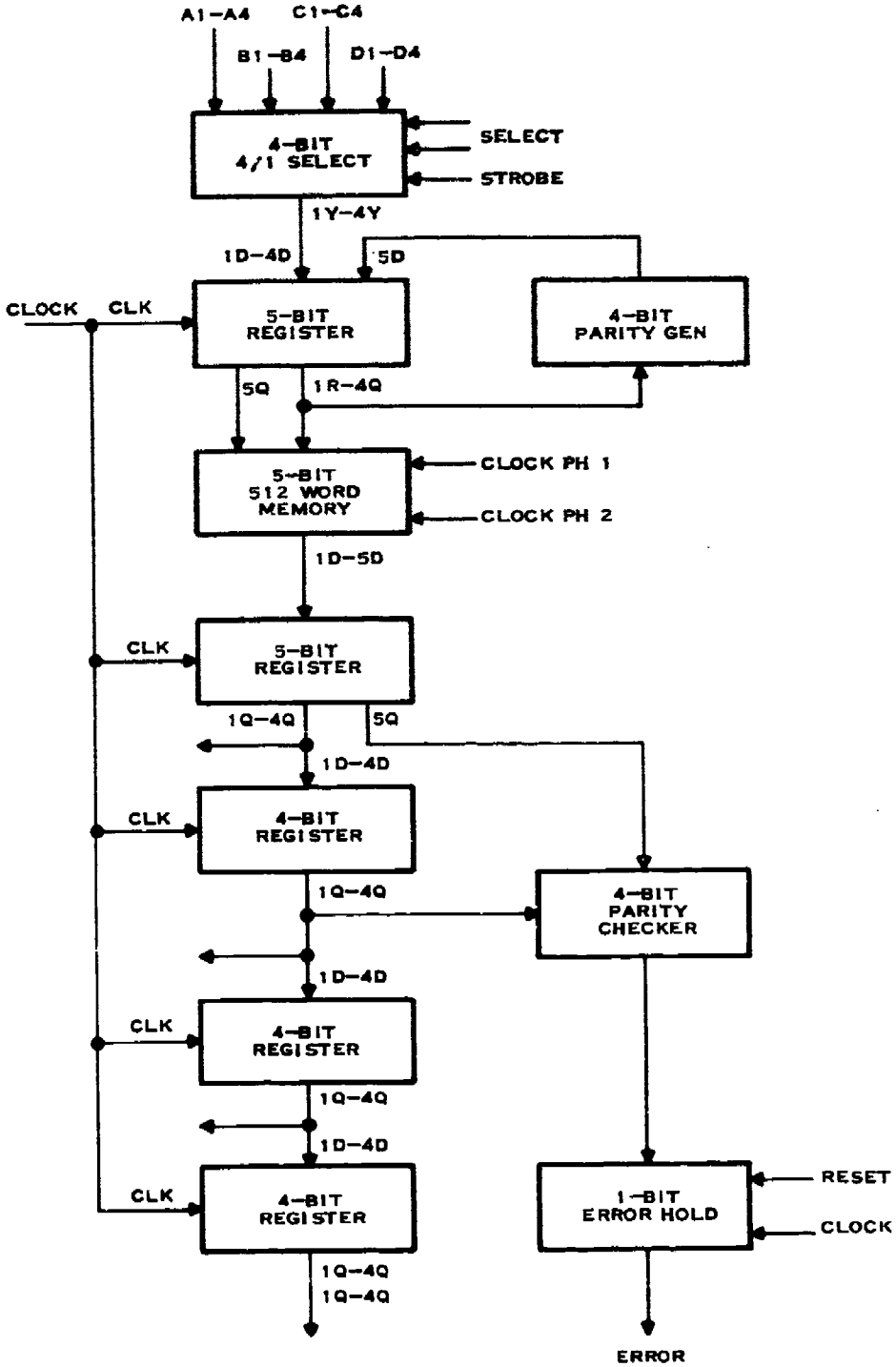

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Figure 42 – Four-Bit Memory Board.

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

SELECT INPUTS A AND B ARE COMMON TO BOTH SECTIONS.

H = HIGH LEVEL, L = LOW LEVEL,
X = IRRELEVANT

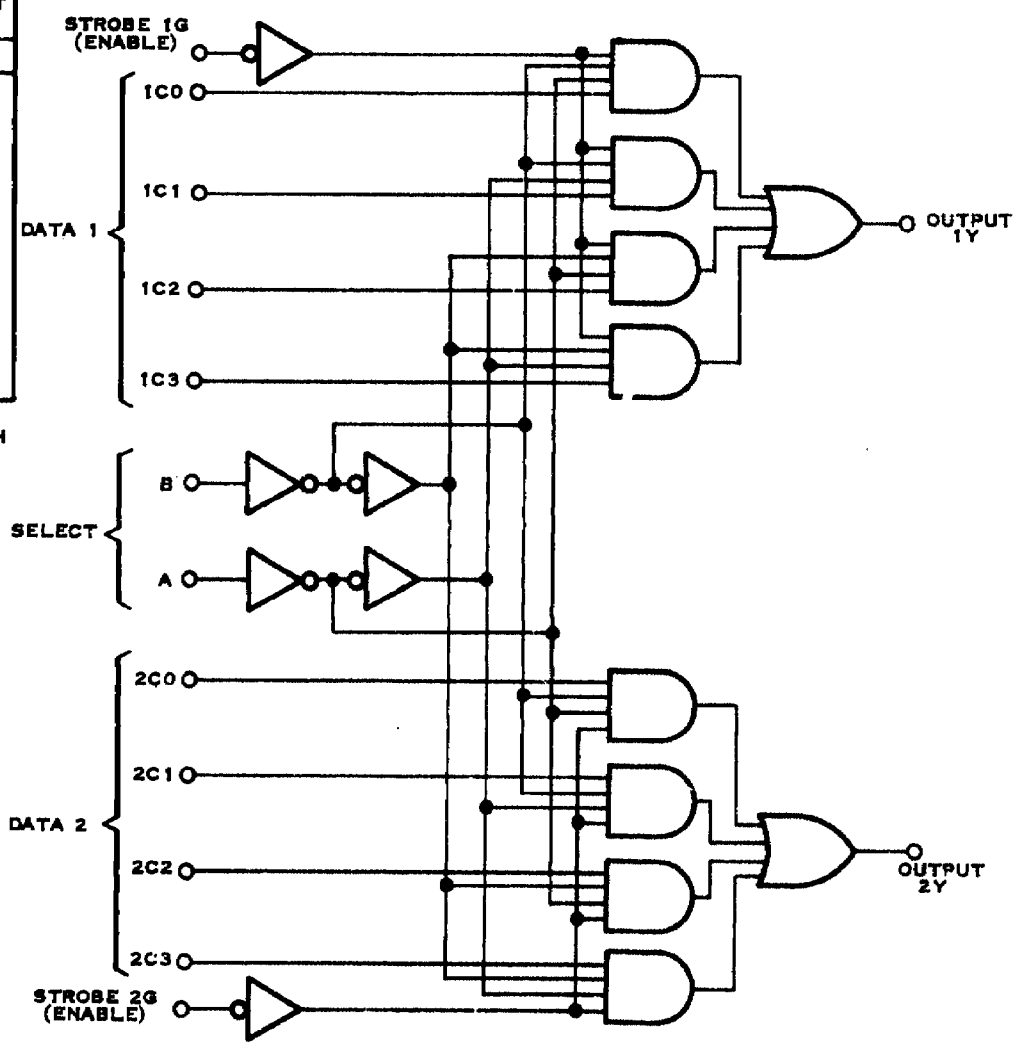

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Figure 43–Logic Function Table and Diagram.

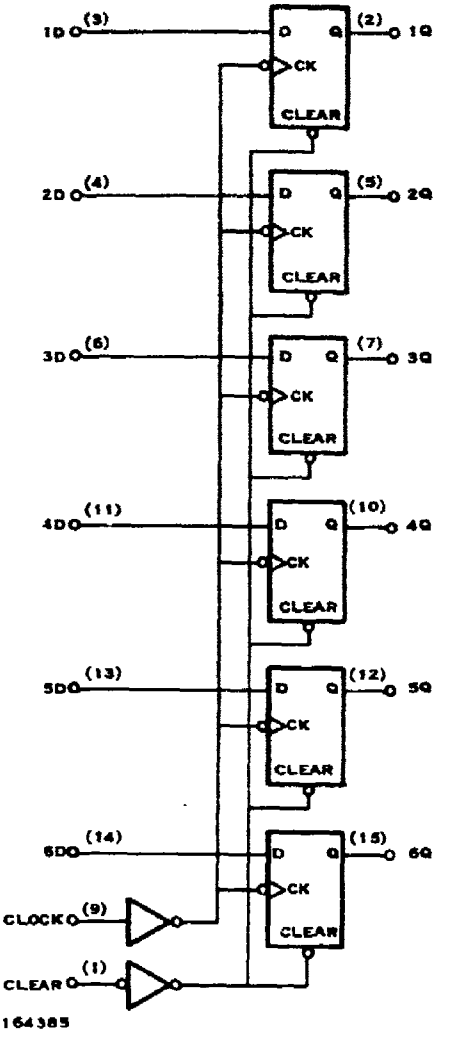

Figure 44–Typical Six-Bit Register.

The parity generator/checker comprises a series of exclusive or logic circuits interconnected to form either even or odd parity. The EVEN IN control is grounded for odd parity generation. The parity bit is connected to the ODD IN control and its inverse connected to the EVEN IN control for odd parity check which is indicated by the ODD OUTPUT. The logic function diagram is shown in Figure 45.

The shift register memory comprises a series of dynamic shift registers connected to form the desired number of bits. The logic function diagram for a 1-bit width by 512-word length memory is shown in Figure 46.

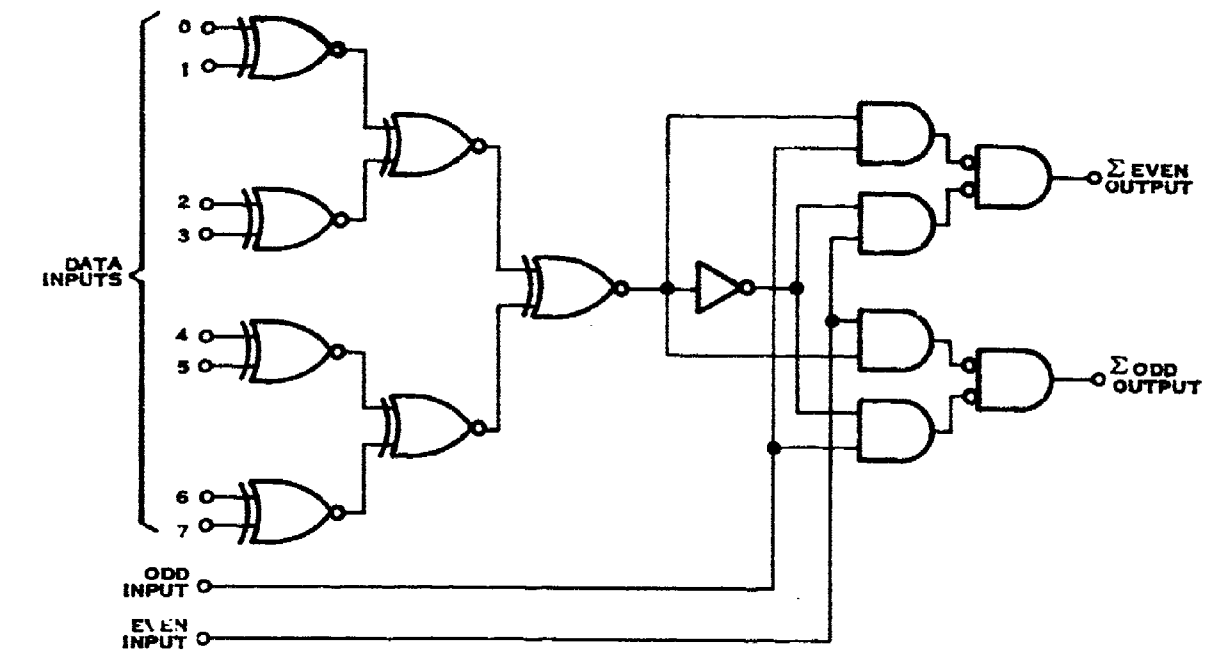

Figure 45 – Parity Generator/Checker Logic Function.

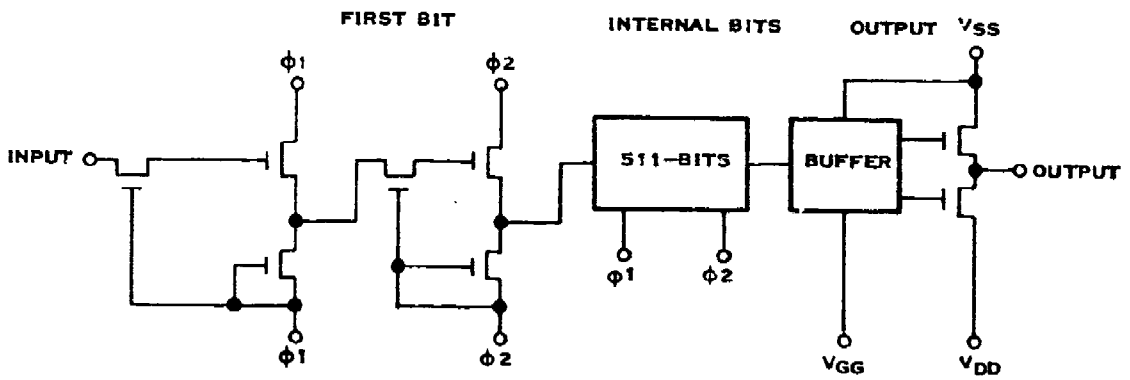

Figure 46 – One-Bit Width by 512 Word Length Memory Logic Function.

Name: Constraint Memory Board #1

Special: X | Family: Digital

Repairable: No | Span: 2, Thickness: A

Functionally Specified: X

Environment: Class I

Power Dissipation: 4.5 watts

Power Requirement: +5 Vdc, −12 Vdc

FUNCTION DESCRIPTION AND DIAGRAM

This module comprises one 16-bit 2-line-to-1-line data selector, one 18-bit register, two 8-bit parity generators, and one 18-bit by 32-word shift register memory with appropriate pull-down resistors for direct interface with standard TTL circuits.

Figure 47 is a block diagram of constraint memory board No. 1. Parameters are given in Table 22.

TABLE 22 – CONSTRAINT MEMORY BOARD NO. 1.

Parameter	Minimum	Typical	Maximum	Units
Operating Frequency	0		3	MHz
Operating Temperature	0		70	°C
Input Threshold Voltage				
(a) Logic "0"	2			V
(b) Logic "1"			0.8	V
Output Voltage				
(a) Logic "0"			0.4	V
(b) Logic "1"	2.4			V
Supply Voltage	4.75	5	5.25	V
		−12		V
Supply Current		548		mA at 5 V
		20		mA at −12 V
Power Dissipation (50-Percent duty cycle)		3.0		Watt

The 2-line-to-1-line data selector comprises a series of gates interconnected to perform the data selection function with control from both a strobe line and select line. The logic function table and diagram are given in Figure 48.

The registers comprise a series of D-type flip-flops connected for parallel-input and parallel-output operation. The number of flip-flops is extended to the desired register length. A typical 6-bit register is shown in Figure 49.

The parity generator/checker comprises a series of exclusive or logic circuits interconnected to form even or odd parity. The EVEN IN control is grounded for odd parity generation. The parity bit is connected to the ODD IN control and its inverse connected to the EVEN IN control for odd parity check which is indicated by the ODD OUTPUT. The logic function diagram is shown in Figure 50.

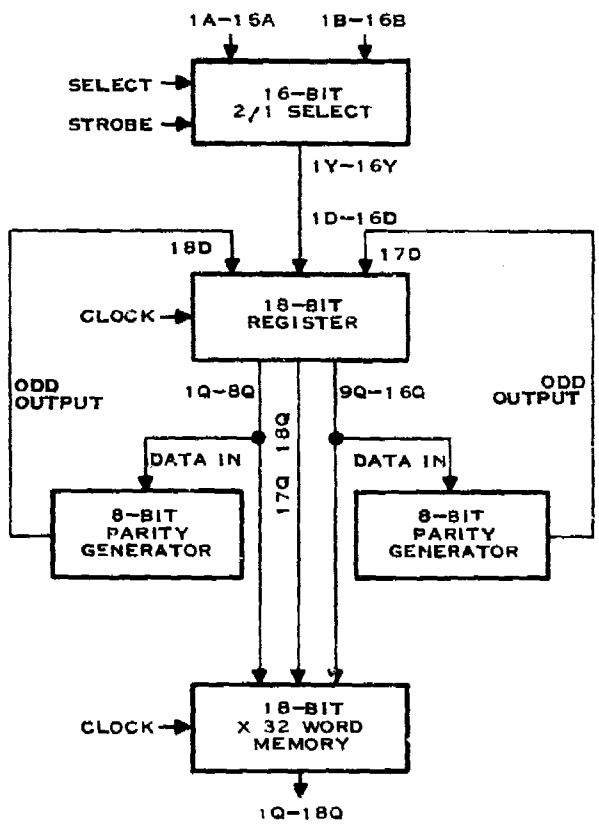

Figure 47 – Constraint Memory Board Number One.

FUNCTIONAL TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH LEVEL, L = LOW LEVEL,
X = IRRELEVANT

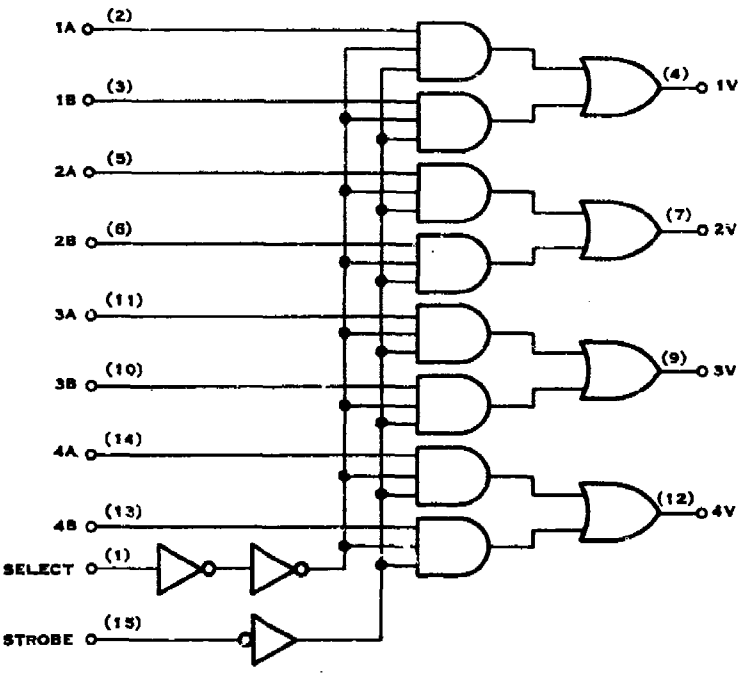

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Figure 48 – Two-Line-to-One-Line Data Selector.

The adders comprise a series of 4-bit binary full adders with full-carry look-ahead connected in cascade to extend the adder bit length to the desired length. A typical 4-bit adder diagram is shown in Figure 51.

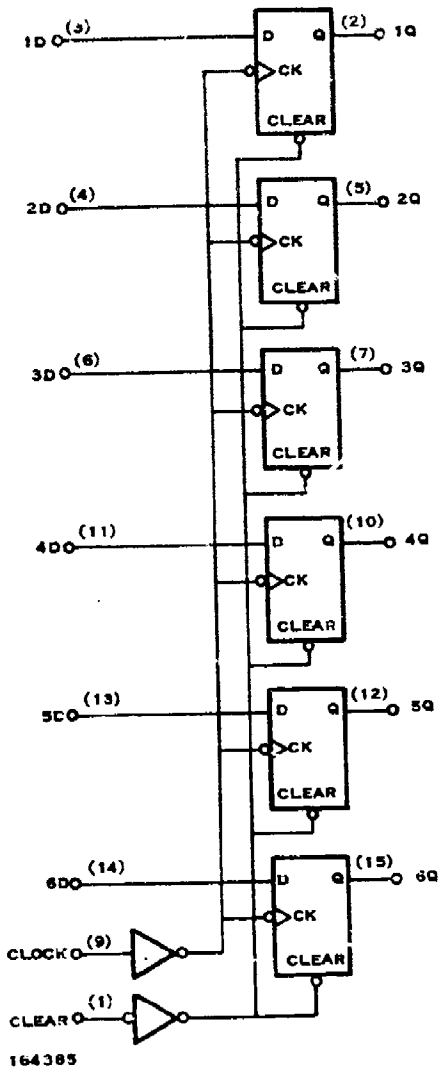

Figure 49–Typical Six-Bit Register.

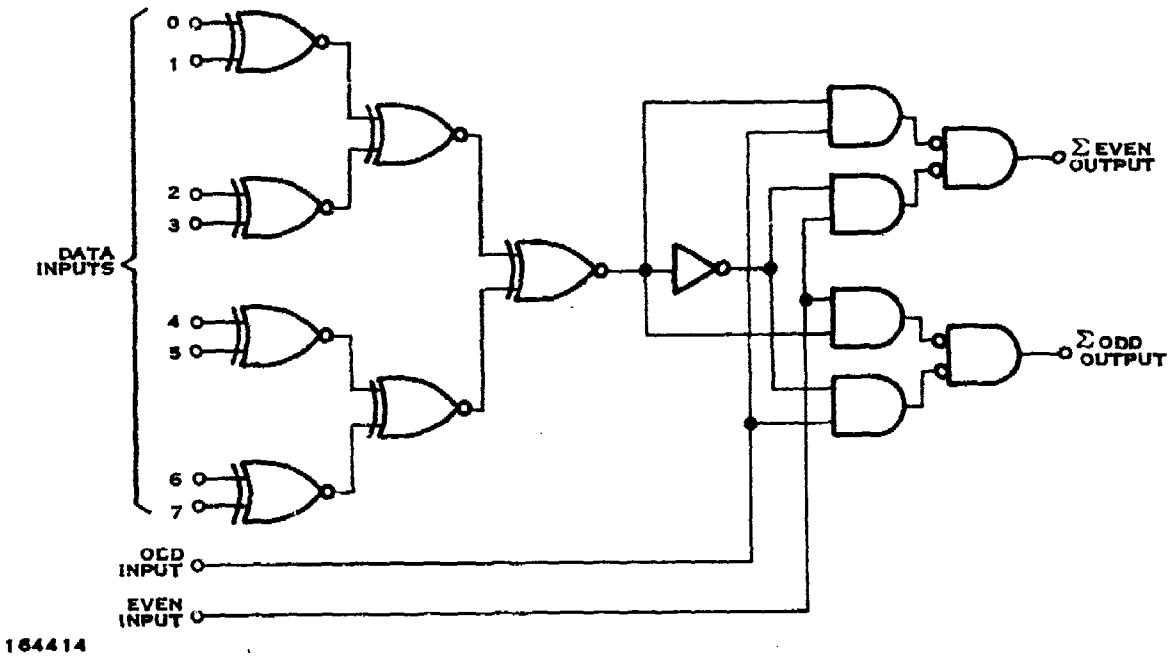

Figure 50 – Parity Generator/Checker Logic Function Diagram.

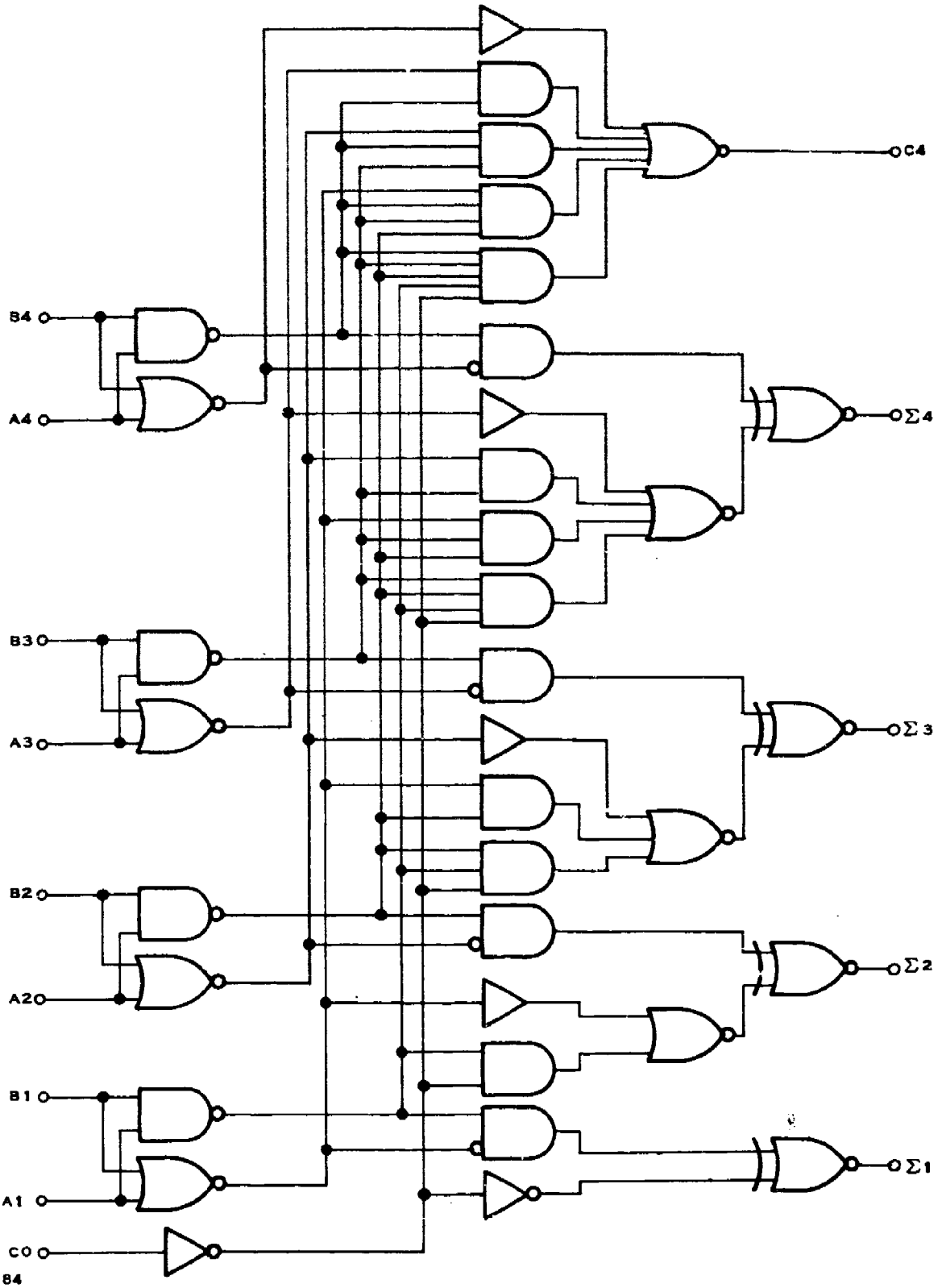

Figure 51 – Four-Bit Adder Diagram.

Name: Constraint Memory Board #2

Special: X | Family: Digital

Repairable: No | Span: 2, Thickness: A

Functionally Specified: X

Environment: Class I

Power Dissipation: 5.17 watts

Power Requirement: +5 Vdc

FUNCTION DESCRIPTION AND DIAGRAM

This module comprises one 18-bit register, one 16-bit register, two 8-bit parity checkers, and one 16-bit full adder with overflow detection capability.

The constraint memory board No. 2 is shown in Figure 52. Parameters are given in Table 23.

TABLE 23 – CONSTRAINT MEMORY BOARD NO. 2.

Parameter	Minimum	Typical	Maximum	Units
Operating Frequency	0		4	MHz
Operating Temperature	0		70	°C
Input Threshold Voltage				
(a) Logic "0"	2			V
(b) Logic "1"			0.8	V
Output Voltage				
(a) Logic "0"			0.4	V
(b) Logic "1"	2.4			V
Supply Voltage	4.75	5	5.25	V
Supply Current		690		mA
Power Dissipation (50-Percent duty cycle)		3.45		Watt

The registers comprise a series of D-type flip-flops connected for parallel-input and parallel-output operation. The number of flip-flops is extended to the desired register length. A typical 6-bit register is shown in Figure 53.

The parity generator/checker comprises a series of exclusive or logic circuits interconnected to form even or odd parity. The EVEN IN control is grounded for odd parity generation. The parity bit is connected to the ODD IN control and its inverse is connected to the EVEN IN control for odd parity check which is indicated by the ODD OUTPUT. The logic function diagram is shown in Figure 54.

The adders comprise a series of 4-bit binary full adders with full-carry look-ahead connected in cascade to extend the adder bit length to the desired length. A typical 4-bit adder diagram is shown in Figure 55.

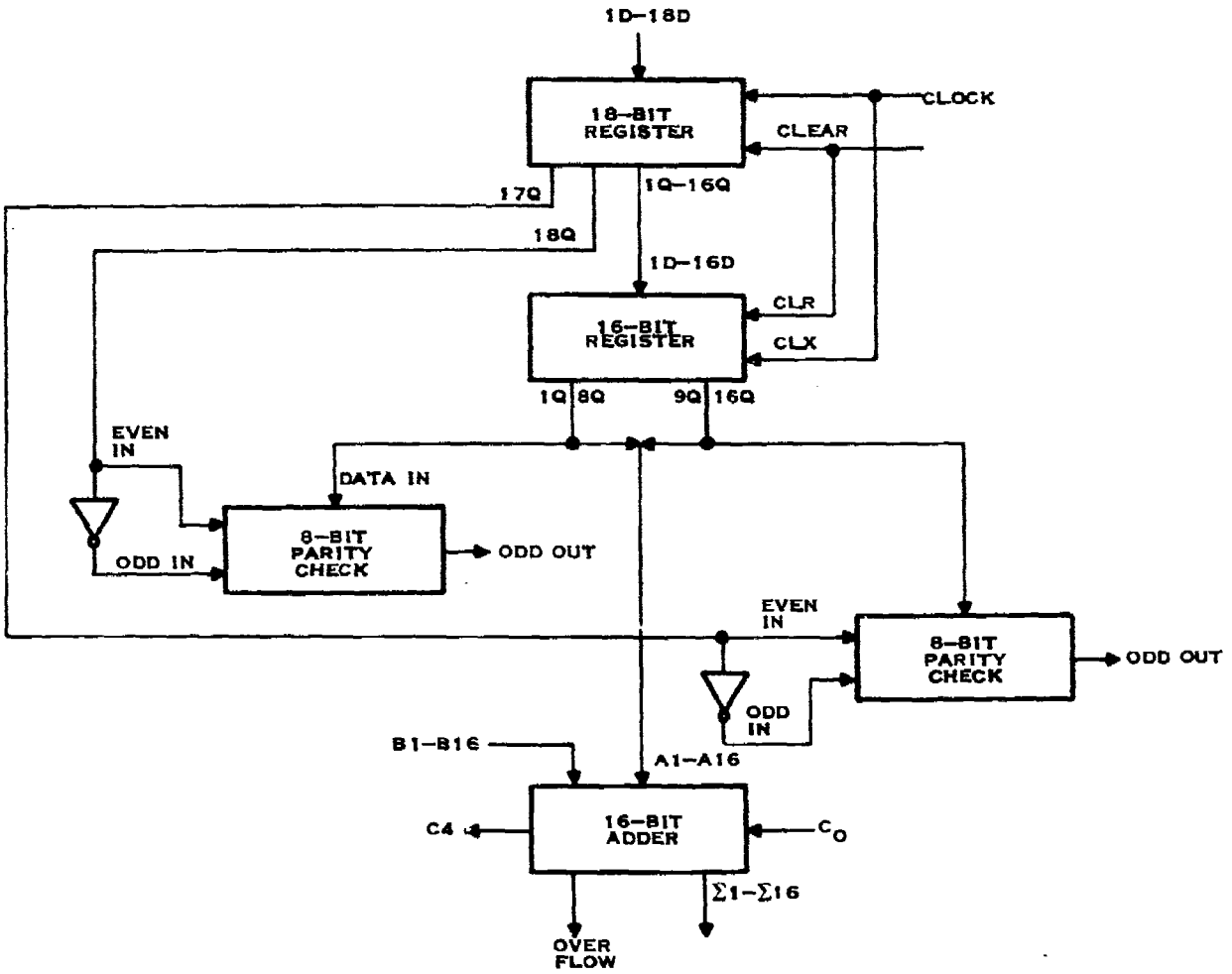

Figure 52–Constraint Memory Board No. 2.

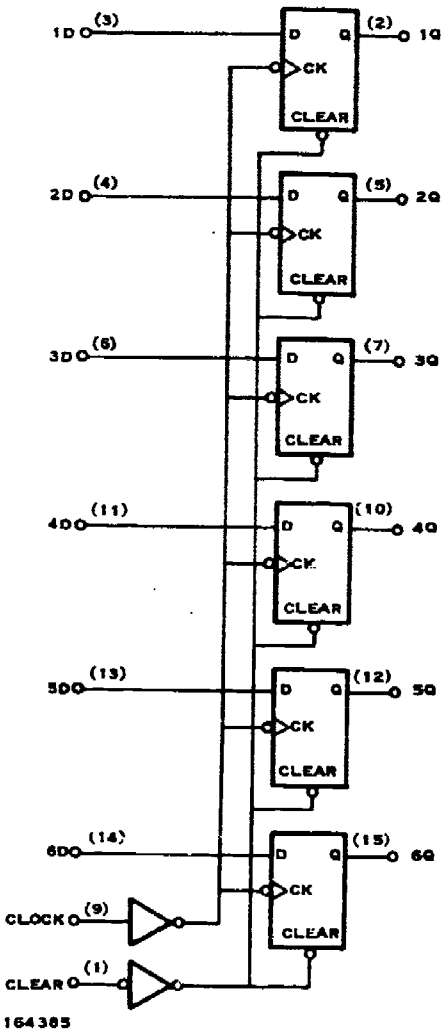

Figure 53–Typical Six-Bit Register.

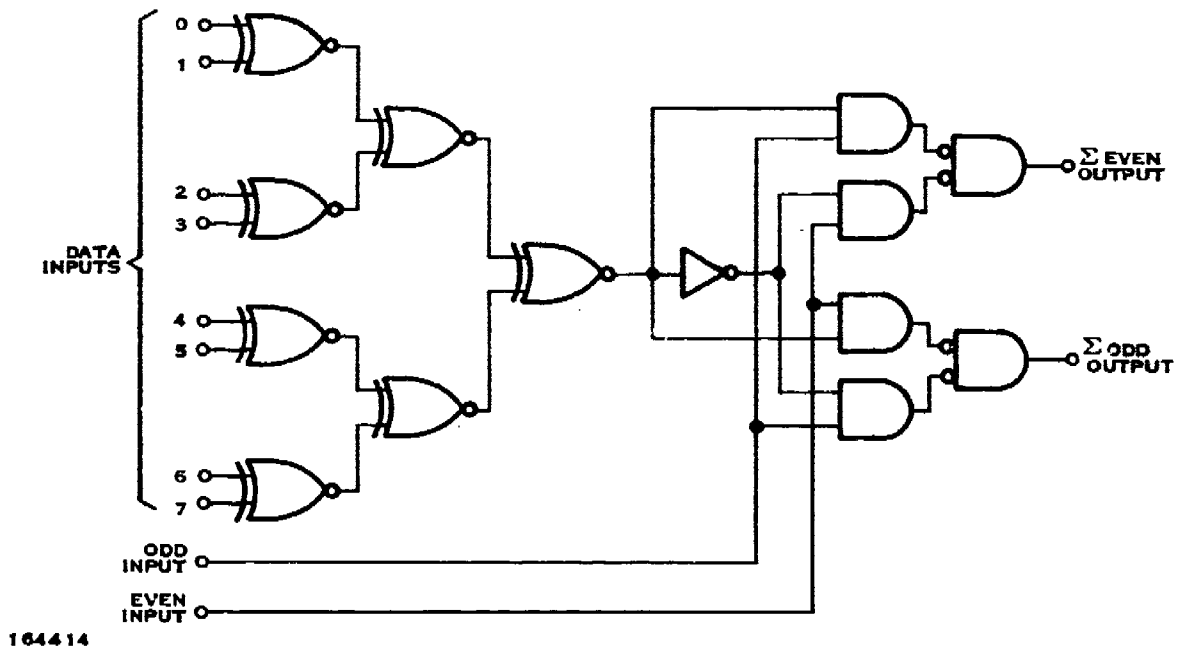

Figure 54–Constraint Memory Board Logic Function.

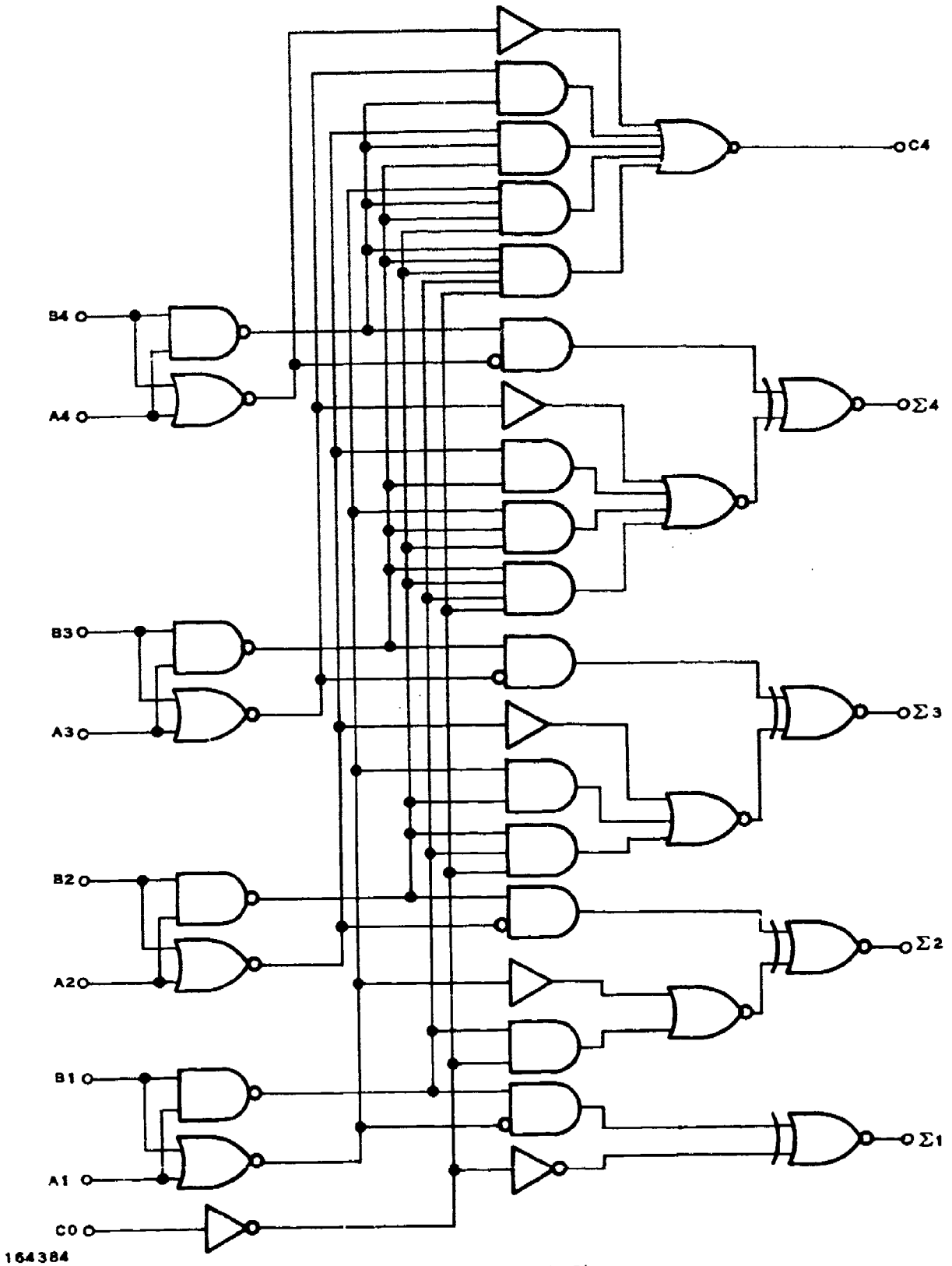

Figure 55–Typical Four-Bit Adder Diagram.

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The following documents are referred to in the text:

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5. *Adaptive Beamforming (ABF) Systems Designer's Handbook*, Interim Engineering Report No. 3, Texas Instruments Incorporated, 12 March 1973.

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13. ABSTRACT

This Final Engineering Report summarizes the results of a study conducted for the Navy to develop an Adaptive Beamforming (ABF) Systems Designer's Handbook to aid sonar system planners and designers in conducting tradeoff analyses of such variables as size, weight, power and complexity versus system capability. Tasks involved in this study which are summarized in this report include algorithm definition, system design, semiconductor tradeoff analyses, system implementation, and handbook and module specification generation. Summary charts and equations relating design parameters to system size, weight, power, and complexity are conveniently tabulated in appendix form for ease of use by the sonar system designer.

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